Aswan Faculty of Engineering
Aswan University

Design of CMOS Integrated High Performance DC-DC Converter for Low-Power Processor Applications

By
Mohamed Saad
B. Sc., Electrical Engineering, South Valley University, 2008

A thesis submitted in partial satisfaction of the requirements for the degree of
Master of Science
In
Electrical Engineering
From
ASWAN UNIVERSITY
EGYPT

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This thesis is dedicated to my parents for their love, encouragement and endless support. They have been my constant source of inspiration

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June 2012

Abstract

Many of appliances that we used daily in our life, include chips fabricated with the most advanced semiconductor technology. An example for these chips is the microprocessor. Microprocessor is more loaded by tasks and functions than any other chip in the portable devices. Current trend in the market is to decrease the supply voltage for such microprocessors to effectively manage their power. Add to this, the increased functionality of microprocessors make them in need for high current. This puts more challenges in the design of power supplies for microprocessors.

It is necessary for the designer to improve the efficiency of the power supply for the embedded microprocessor to extend the battery life. Even improving the efficiency of the power supply is a crucial requirement; the size and cost are other important issues that should be taken into account.

This thesis gives an overview about the importance of the power supply for recent microprocessors and the types of voltage regulators available in the market. A study on the available power architectures for microprocessors is presented, and then the two-stage power architecture is proposed and designed to replace the old regulator.

This thesis discusses the design of two types of power supplies; switched-capacitor converters and synchronous buck converter. The design of building blocks for converter is also presented. Then, each stage is simulated individually and simulation results are given.

The synchronous buck converter is fabricated using 0.25µm CMOS process and experimental results are shown. The experimental results show that an average efficiency higher than 90% is obtained from the first stage individually.

For higher efficiency, two-stage architecture is proposed based on the two power converters. The first stage is a switched capacitor converter and the second stage is a synchronous buck converter. The two-stage system is integrated and the efficiency of the total system is simulated and compared to the efficiency of two selected market examples. The comparison showed that the two-stage approach has better efficiency than the one-stage approach.

Finally, for better transient response, a novel linear-nonlinear control technique is proposed to enhance the transient response of the regulator during load transient. The linear-nonlinear control is applied to the two-stage converter which yields a high performance converter that can be used for modern low-power microprocessors.

Content

List of Figures

List of Abbreviations

AC	:	Alternating Current
BJT	:	Bipolar Junction Transistor
CCM	:	Continuous Conduction Mode
CMOS	:	Complementary Metal Oxide Semiconductor
CPU	:	Central Processing Unit
CTAT	:	Complementary to Absolute Temperature
DCM	:	Discontinuous Conduction Mode
DCR	:	DC Resistance
DSC	:	Digital Still Camera
EA	:	Error Amplifier
EMI	:	Electromagnetic Interference
ESR	:	Equivalent Series Resistance
ESL	:	Equivalent Series Inductance
FET	:	Field Effect Transistor
HS	:	High Side FET
HV	:	High Voltage
IBM	:	Intermediate Bus Architecture
IC	:	Integrated Circuit
LHP	:	Left Half Plane
LNL	:	Linear-Nonlinear
LS	:	Low Side FET
LV	:	Low Voltage
NCT	:	Nonlinear Control Technique
NOM	:	Nonlinear Operation Monitoring
Op Amp	:	Operational Amplifier
PA	:	Power Amplifier
PC	:	Personal Computer
PCB	:	Printed Circuit Board

PDA	:	Personal Digital Assistant
PFM	:	Pulse Frequency Modulation
PMIC	:	Power Management Integrated Circuit
POL	:	Point of Load
PTAT	:	Proportional to Absolute Temperature
PUPS	:	Point of Use Power Supply
PWM	:	Pulse Width Modulation
RF	:	Radio Frequency
RHP	:	Right Half Plane
SCC	:	Switched Capacitor Converter
SMPS	:	Switch Mode Power Supply
SoC	:	System on Chip
SPDT	:	Single Pole Double Throw
SW	:	Switching Node
UGB	:	Unity Gain Bandwidth
VID	:	Voltage Identification
VM	:	Voltage Mode
VRM	:	Voltage Regulator Module

Chapter 1

Introduction

- ***Evolution in Power Management ICs***
- ***DC-DC Converter***
- ***Power Management Devices Overview***
- ***Moore's Law and Power Supply Challenges***
- ***Motivation***
- ***Thesis Organization***

Chapter 1

Introduction

1.1 Evolution in Power Management ICs

Throughout the hours of our day, there are a large number of devices and appliances that we use. Every time and every day you can see people talking in their cellular phones, listening to music on their iPod, searching the web and chatting using laptops. When you decide to go to trip, you can see most of your friends listening to their MP3 player and taking photos with their digital cameras. In addition, the days are gone when a camera was only a camera, an MP3 player was only an MP3 player, and a phone was only a phone. Nowadays all these appliances can be found in one appliance.

Many of the last appliances include chips fabricated with the most advanced semiconductor technology. These chips are expected to become smaller to the extent that enable it to be embedded at any portable device and can perform more and more functions. Thanks to CMOS technology scaling, the feature size of the transistor at a specific technology can be reduced. This means that for the same number of transistors in a chip, the physical area can be significantly reduced.

In addition, these appliances are portable electronic equipment and thus they are battery-powered which require chips with the lowest power consumption to maximize the battery run-time. One of the most effective

ways is to run these chips at the lowest possible supply voltage. Reducing the supply voltage is a big benefit emerged from CMOS scaling. In portable electronic equipment, high-efficiency power management IC (PMIC) is required to efficiently manage the voltage and current from a single battery source.

PMICs can contain battery management, voltage regulation, charging and DC-DC converters among other functions.

As the semiconductor products going to be light, small, and multi-function, the area occupied by PMICs becomes more and more important.

PMICs constitute a large portion of the "voltage regulator" revenues, and the continued growth in market size is shown in Fig. 1-1. The growing demand of portable applications, the volume of which is consumer driven, is a large component of this growth [1].

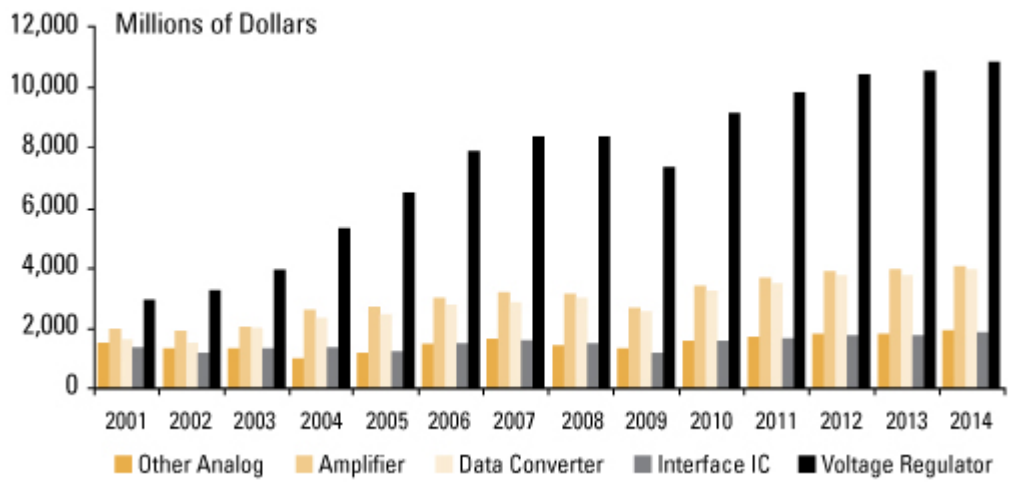


Figure 1- 1: Analog IC revenue by type [1].

Due to this continued growth in market, two trends have emerged. One is for lower cost, simple PMICs, many of which are being integrated into their host IC's package, thus becoming a System on-Chip (SoC). These devices serve very basic features.

The other trend is to have more complex PMICs that become part of the chipset of the application. Examples of this are feature-rich cellphones or mobile computing devices. Another continuing trend pertaining to the functional technology of PMICs is improving efficiency to extend the battery life of the mobile appliances that the PMICs are used in.

Focusing on voltage regulation and DC-DC converters, they constitute most of the PMICs market and pose large attention at any consumer device.

1.2 DC-DC Converters

DC-DC converters are electronic devices used whenever we want to change DC electrical power efficiently from one voltage level to another. Often, they are called "*Power Supplies*". They are needed because unlike AC, DC cannot simply be stepped up or down using a transformer. In many ways, a DC-DC converter is the DC equivalent of a transformer.

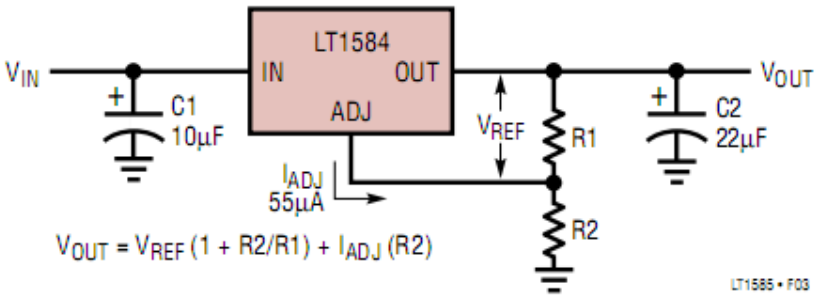
While DC-DC converters can be categorized into many types, they can be classified depending on method of conversion. The two basic methods are linear voltage converters and switch-mode power supply:

1.2.1 Linear Voltage Converters

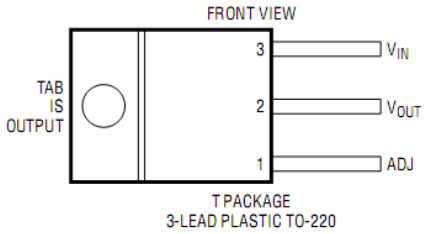
The most elementary DC-DC converters are linear voltage converters. Linear converters can only have output at lower voltages from the input. Their operation is depending on active devices. Active devices can be BJTs or FETs with these active devices operating in their linear region.

The active device acts like a variable resistor in its linear region. The variable resistor is continuously adjusted to maintain a constant output voltage. Linear regulators achieve DC-DC voltage conversion by dissipating the excess power into device's resistance. Clearly, they are inefficient when the voltage drop is large and the current is high as they dissipate heat equal to the product of the output current and the voltage drop; consequently they are used for limited applications where the voltage drop and current is not large.

Linear regulators are inexpensive, reliable at low-power applications, simpler of any other DC-DC converter. They can provide low-noise output voltage; hence they are suitable for powering noise-sensitive low-power applications such as radio frequency (RF) circuits. Linear regulators are available commercially in the form of three-terminal TO220 packages and TO236 packages. An example for linear regulator IC is LT1585 from Linear Technology [2].



(a) Basic adjustable regulator.



(b) TO220 package.

Figure 1-2: LT1584 - 7A fast response positive adjustable regulators (Linear Tech) [2].

1.2.2 Switch-Mode Power Supplies

Switch mode power supplies (SMPS) convert one DC voltage level to another. The idea of conversion depends on storing the input energy temporarily and then releasing it to the output. The energy storage may be in either magnetic field storage element (such as inductor or transformer) or electric field storage element (such as capacitor). Unlike linear regulators, the pass element of SMPS switches very quickly at a predetermined switching frequency between on and off-states. The value of the output voltage relays on the ratio of on to off time. In contrast to linear regulators, switch-mode converters are more power efficient. They don’t dissipate the

unwanted power in the form of heat. This makes them brilliant for applications where high efficiency is a highly required.

SMPSs are more complicated and their switching currents can cause electrical noise which may cause electromagnetic interference (EMI) problems which make them not suitable for noise-sensitive applications such as RF communication systems. They are, however, still excellent replacement for linear regulators when high efficiency is required.

SMPSs basically have two types in accordance to their storage element. The two types are as following:

1.2.2.1 Magnetic (Inductive) Type

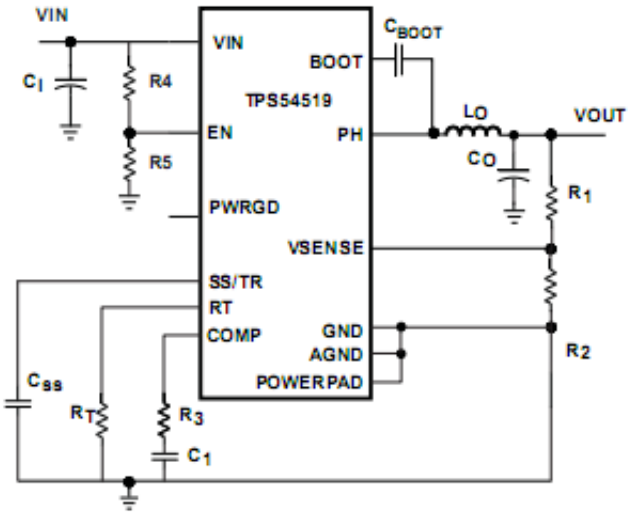
This type uses magnetic component such as inductor or transformer as a storage element. The energy is stored and released in a periodic way using the magnetic field of the inductor or transformer. The on/off time ratio (duty cycle) of the charging voltage is adjusted which adjusts the amount of power transferred.

The inductive SMPS can be classified into isolated and non-isolated topologies. All the isolated topologies include a transformer and thus can produce an output of higher or lower voltage than the input by adjusting the turns ratio. The non-isolated topologies are simpler. They are used where the voltage needs to be stepped-up or down by a relatively small ratio, and there is no problem with the output and input having no dielectric isolation. There are three basic non-isolated SMPS topologies: the buck (step-down), the

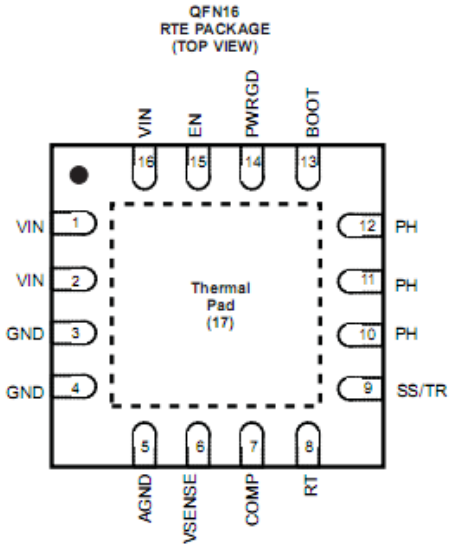
boost (step-up) and the buck-boost (inverting). The function of each topology can be described as following:

- Buck (step-down) converters: are used to produce an output voltage between ground and the input voltage.
- Boost (step-up) converters: operate in the opposite manner compared to the step-down converters generating higher voltage at the output than at the input.
- Buck-Boost converters: are used in applications where the output voltage is required to have levels both higher and lower than the input voltage.

The inductive type SMPS is available commercially for the three basic SMPS topologies. Fig. 1-3 shows an example for commercial buck SMPS.



(a) Typical application circuit.



(b) QFN16 RTE Package.

Figure 1-3: TPS54519 – 5A synchronous step-down SWIFT converter [3].

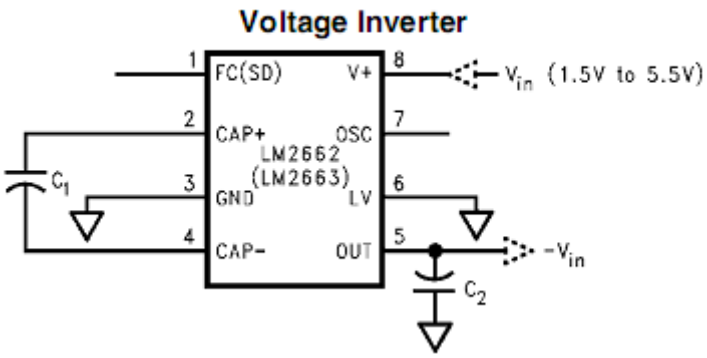
1.2.2.2 Capacitive Type

The capacitive SMPS theory of operation depends on the electric filed stored on one capacitor or few number of capacitors. The core circuit of capacitive SMPS is composed of switches and a few capacitors, traditionally called “flying capacitors”, used for storing and transferring energy. By turning-on and turning-off switches to change the connection of flying capacitors, these capacitors can be charged or discharged and the charges can be delivered to or removed from the output.

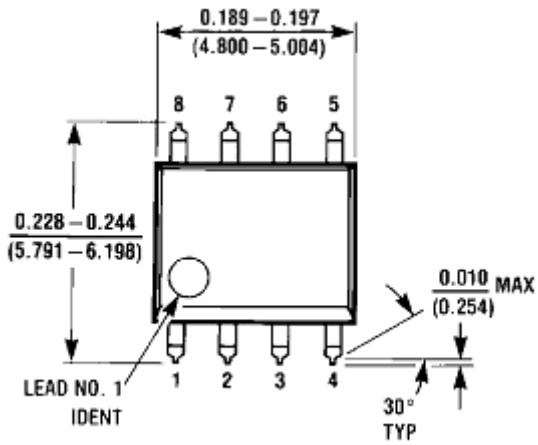
By alternately connecting capacitors to the input and output in different ways, different topologies can be obtained. The capacitive SMPS is commercially called “switched-capacitor converters”. They are also sometimes referred to as charge pump converters.

They are typically used in applications requiring power conversion functions at relatively small amounts of current. These functions include doubling, halving and inverting the input voltage, and can be combined to achieve other conversion ratios. The standard switched-capacitor converters are often unregulated or supplemented with a linear regulator for voltage regulation.

Owing to the advanced integration techniques, switched-capacitor converters are now available commercially in the form of 8-lead small outline integrated circuit (SOIC) package. An example for commercial switched-capacitor converter is LM2662 which shown in Fig. 1-4 [4].



(a) Basic application circuit for LM2662.



(b) 8-lead SOIC package.

Figure 1-4: LM2662 – Switched capacitor voltage converter (National Semi.) [4].

1.3 Power Management Devices Overview

Successful power conditioning for today's demanding electronic systems is a complex and challenging task. While it is absolutely necessary, power is generally invisible to the system's performance as seen by a potential customer. The power supply is expected to take up no space; contribute no heat; add no cost; and contribute no problems to a system's reliability.

There are three distinct categories of portable devices: (1) PC-based devices characterized by high-current requirements powered by a battery pack, (2) handheld devices (excluding cell phones) characterized by very low-power requirements and a broad range of device types, and (3) cell phones characterized by very low power requirements, highly integrated processor-oriented power management ICs, and a large unit volume [5].

Third generation "smart" cell phones combine the traditional 2G cellular phone with PDA-like features as well as digital still cameras (DSCs) and music players (MP3s). Fig. 1-5 shows a simplified block diagram of a 3G phone with its major subsystems and their respective voltage rails. Such diversity in functionality requires numerous components, most of which have different power rail voltages, with each rail having growing power demands and application-specific requirements. At the same time, consumers want smaller phones with maximum battery life and minimal battery charge time. All of these requirements have driven development of various high performance and/or highly specialized PMICs [6].

Mobile consumer-electronics devices, especially smart phones, are powered from batteries which are limited in size and therefore capacity. These devices integrate diverse functionality as voice communication, audio and video playback, web browsing, short-message and e-mail communication, media downloads, gaming and more. The rich functionality increases the pressure on battery lifetime, and deepens the need for effective energy management [7].

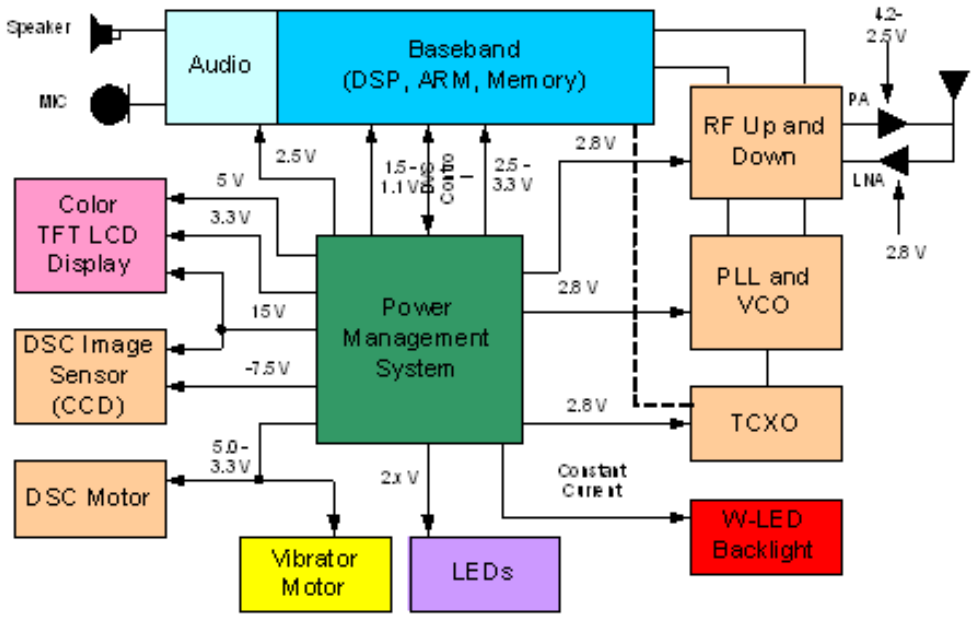


Figure 1- 5: 3G smart phone block diagram [6].

Good energy management requires a good understanding of where and how the energy is used. The most power consuming components are the digital baseband and CPU. Knowing the most power consuming component at any system would help us in exerting more efforts and a lot of care during the design of its power supply.

1.4 Moore's Law and Power Supply Challenges

More than 25 years ago, Gordon Moore forecasted the rapid pace of silicon technology. Moore predicted that the number of transistors on a chip roughly doubles every two years. Moore's observation became a well-known description of progress in integrated electronics.

The increasing demand for computing and communication devices to be used in every aspect of life resulted in the need for smaller processors that can be embedded at any portable device and can perform more and more functions. This gives the chance to *process scaling* revolution. Based on the technology scaling, the feature size of the transistor at a specific technology can be reduced. By using smaller and smaller transistors, more complex circuits can be used within the die space budget. This equates to more cache, larger buffers, more execution units, or even multiple cores on one die. Also, technology scaling allows for faster circuits and this is why smaller process leads to increase in clock speed. All of the previous benefits are following Moore's prediction.

For better power management, smaller power consumption and hence less heat, the processor voltage needs to be scaled too. Fig. 1-6 shows the effect of scaling voltage and increasing frequency on power consumption of a processor.

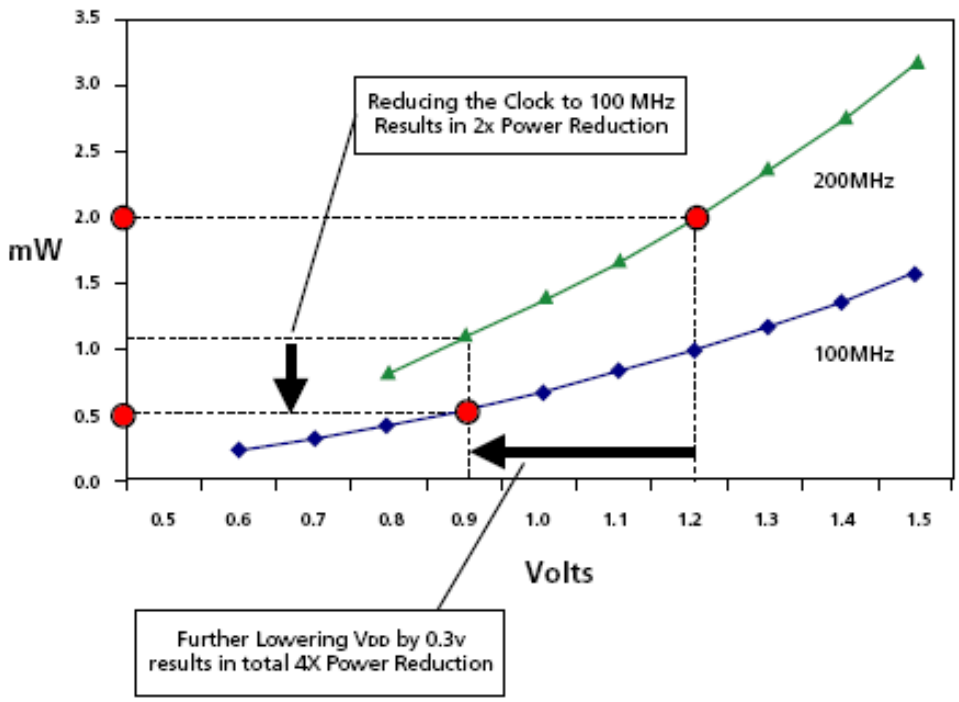


Figure 1- 6: Effects on power of varying voltage and frequency [9].

The processor supply voltage in future generation processors is decreased from 3.3 V to 1.1 V and smaller. Meanwhile, because more devices are packed on a single processor chip and the processors operate at higher operating frequencies, microprocessors need aggressive power management. Future generation processors' current draw will increase from 13 A to 30 A 50 A [8]. It is a big challenge for processors power supply to efficiently produce low voltages under high current loads.

A good example for such low-power processors is Intel Atom ™ processor. Intel Atom ™ processor is a low-power general purpose processor that powers a variety of devices such as tablets, smartphones, netbooks, hybrids, consumer electronics, and entry-level desktop PCs. Compared to Intel Pentium 2 Xeon, which consumed about 40 W of power nearly 10 years

ago, the current generation of Atom ™ processor consumes 3 to 5 W with about twice the compute performance [10]. Fig. 1-7 shows a summary for the power needs of Intel Atom ™ processor families and the launch year of each family.

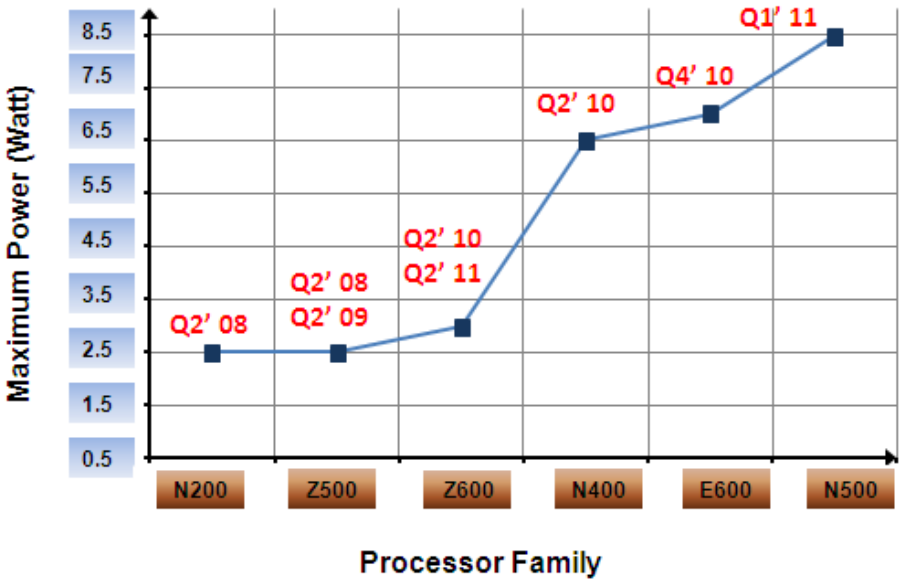


Figure 1- 7: Maximum power needs for Intel Atom processor families [11].

As shown in Fig. 1-7, the power needs of Intel Atom families are increased every year according to the increased demand for higher speeds and more functionality. Most of these processor families are operating at very low voltage that ranges from 0.75 V – 1.2 V and require a relatively high current that can reach 7 A and higher (as for Atom N500 series).

1.5 Motivation

Current trends in consumer electronics demand diverse functionality. Our smartphone is a good example that we can consider. For our smartphone to communicate faster, capture very high resolution photos, display HD videos and movies, read PDF files, and sending files via wireless or Bluetooth connection; it needs a very fast and advanced processor embedded on it.

For a processor to do all of these functions and be able to make more than one function at the same time as well; it must be fabricated using the most advanced and recent technologies. The recent technologies used in fabricating such processor decrease the supply voltage as an important demand for efficient power and thermal management. Real values for supply voltage of modern processors range between 0.75 V and 1.2 V. In addition to their very low voltage, these processors require relatively high currents to operate billions of transistors that are integrated on the same chip. It is a big challenge for the processor power supply to efficiently produce the very low voltage required under the loading condition of high current.

The goal of this thesis is to design a high performance DC-DC converter for powering the low-power processor generations. This includes:

- Proposal of two-stage architecture for low-voltage buses.
- The design of the two-stage DC-DC converter and compare its efficiency to commercial products available in market.
- The design of transistor-level circuits of the two-stage DC-DC converter.
- Proposal of novel linear-nonlinear control technique for fast transient buck converter.

1.6 Thesis Organization

To meet the scope of this thesis, the thesis is organized as follow:

Chapter two illustrates a review for switched-capacitor converters and its operation theory. The design steps of a 6 V/3 V switched-capacitor converter are discussed. The sub-blocks used in operating the converter is illustrated and converter is simulated. At the end of this chapter, the simulation result of the converter is illustrated. The efficiency of the converter is tested too.

Chapter three discusses the operation theory of buck converters. The design of 2 MHz buck converter's power-stage and PWM controller is covered. The sub-blocks of PWM controller are discussed and simulation results for each sub-block are illustrated. At the end of the chapter, the power-stage and controller sub-blocks of buck converter is integrated and simulated.

Chapter four discusses efficiency limitations of buck converter when used to power modern microprocessors. To solve its limitations, the two-stage power architecture is proposed by integrating the switched-capacitor converter and buck converter into one power supply. The two-stage power supply is simulated and the efficiency of the overall system is investigated.

Chapter five shows the design of nonlinear control that can be used side-by-side with the conventional PWM control to minimize undershoots and overshoots occur at buck converter output due to load transient steps.

Finally, Chapter six summarizes the thesis conclusion and provides a view for the future work.

Chapter 2

Integrated Switched-Capacitor Converter Design

- ***Introduction***
- ***Characterization Parameters for SCC***
- ***SCC's Structure and Topology***
- ***CMOS Realization of Selected SCC***
- ***Power Losses in SCC***
- ***SCC Power Stage Design***
- ***Design of SCC Controller Blocks***
- ***Summary***

Chapter 2

Integrated Switched-Capacitor Converter Design

2.1 Introduction

In this chapter, the design and analysis of switched-capacitor converter (SCC) will be discussed. A detailed design for every block for the on-chip controller will be illustrated. Finally, a simulation results for the converter will be illustrated based on HSPICE simulator.

2.2 Characterization Parameters for SCC

The performance of SCC has been improved significantly over the years. Most of the approaches used to perform DC to DC conversion are inductor-based DC-DC converters. Depending on the power ratings, the DC-DC converter can be partially integrated or fully-integrated. It is often confused when selecting between the inductor-based converters and capacitor-based converters before designing the power supply. It is very important to determine the most effective parameters that characterize SCCs.

2.2.1 Output Voltage Accuracy

The output voltage accuracy is specified as the tolerance of setting the output voltage for a desired value. It is sometimes specified as "*Output Voltage Tolerance*". It is typically specified for a DC-DC converter as a percentage under nominal input voltage and full load conditions.

For any DC-DC converter, it may be regulated or unregulated. The two approaches are very far from each other and completely different. Output voltage regulation means that there is a closed loop system that monitors the output voltage and continuously modulates the converter power-stage to maintain a constant predetermined output voltage. This operation depends on the internal reference voltage accuracy, the feedback voltage accuracy, and the system voltage loop DC gain. The closed loop DC gain has a significant impact on the DC regulation accuracy.

If the output voltage is unregulated, the output voltage value will change in corresponding to input line and load line. This means that there is no predetermined value for the output voltage and the DC-DC converter roughly generates the output voltage depending on its topology.

Specially talking about SCC, the output voltage cannot be regulated by changing the duty ratio of each switch [12].

2.2.2 Converter Efficiency

Efficiency is an important requirement parameter for battery life issue. A low efficiency results in higher power levels being dissipated within the converter as heat. Converter efficiency is a challenging requirement particularly in low-voltage high-current applications. However, high efficiency is not required only under full load, but over a wide range of load variation. As the operated system may enter in idle mode for a long period, the converter efficiency should be maintained high at light-load as well.

Generally, Inductor-based converters are usually considered more efficient for voltage conversion than SCCs. Usually; SCC contains a number of switches higher than any inductor-based converter. This makes the SCC more resistive than inductor-based converter and the efficiency will be highly affected by conduction losses at higher output current. So, the SCCs are not preferred for point of load (POL) applications where the output current is high.

On the other hand, the maximum efficiency of SCC highly depends on their structures and input voltages. As an example, a voltage divider can achieve very high efficiency when the input voltage is around the double of the required output voltage. But, the efficiency decreases dramatically as the input voltage becomes higher or lower than the ideal input voltage for the converter. However, multi-mode SCCs are now available in the market and can adaptively adjust the conversion ratio to achieve the best efficiency. Fig. 2-1 shows the efficiency of commercial step-down SCC as a function of input voltage.

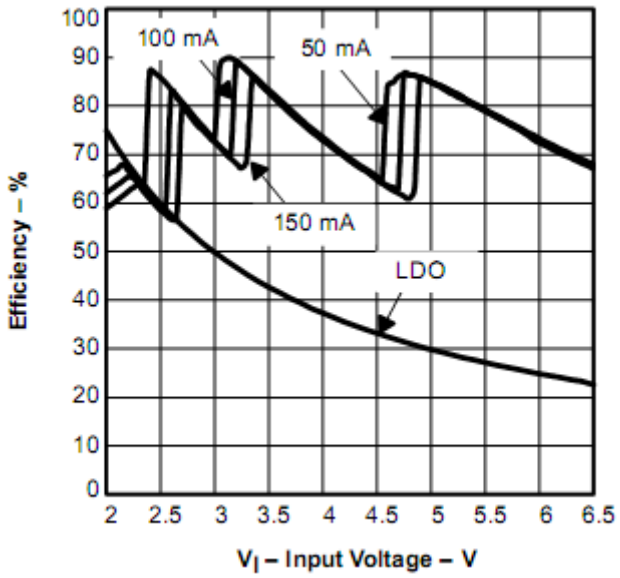


Figure 2- 1: Efficiency vs. input voltage of TPS60500- high efficiency step-down charge-pump [13].

2.2.3 Size and Cost of the Converter

The size of DC-DC converter is one of the most pressing considerations in selecting between different converter circuits. System designers often want the most power in the least size.

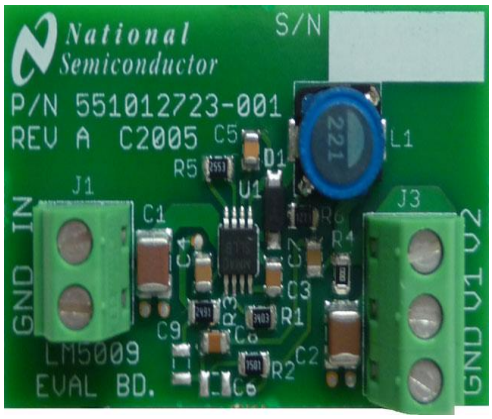
Passive components used in DC-DC converters play key role in determining the overall size of the converter chip. In inductive switch-mode DC-DC converters, it is the inductor that usually dominates the size of the converter. Often, the inductor used in DC-DC converters takes larger area than the IC converter.

SCC has no inductor which gives it a great advantage than inductor-based converters. For this reason, SCCs are ideal for mobile fun-lighting, flash-lighting and torch applications where the area is limited.

Indeed, the challenge is not just to reduce PCB area, but also the profile (height) of the components on the board. In total, the PCB area requirement of a SCC will generally be between 30% and 50% smaller than the area required by a coil converter [14].

Fig. 2-2 shows the evaluation boards of a SCC and buck converter. It is clear from the figure that the buck converter takes larger PCB area than SCC.

(a) Evaluation board of LM3354 Regulated 90mA Switched-Capacitor Converter [15].



(b) Evaluation board of LM5009 100mA synchronous buck converter [16].

Figure 2-2: Evaluation boards of LM3354 and LM5009.

2.2.4 Ripple and Noise of the Converter

Ripple in DC-DC converters can be described as disturbance occurs at the converter output at a fundamental switching frequency. In inductor-based SMPS many parameters can affect the output ripple such as the switching frequency, the duty cycle, output inductor value and output capacitor value.

Additional noise is generated around the resonance frequency of the LC filter and it is usually located within the audio or video frequency range in portable applications [17].

SCC only depends on the capacitors to store its charge. Obviously, the output voltage ripple of such converters can be reduced by increasing the output capacitor value. SCC is similar to inductive SMPS in generating a ripple around the switching frequency of the converter. SCC has a good advantage over the inductive switching converter which is the lake of noise generated by the LC resonance frequency. Fig. 2-3 shows the intrinsic noise of inductive and SCCs.

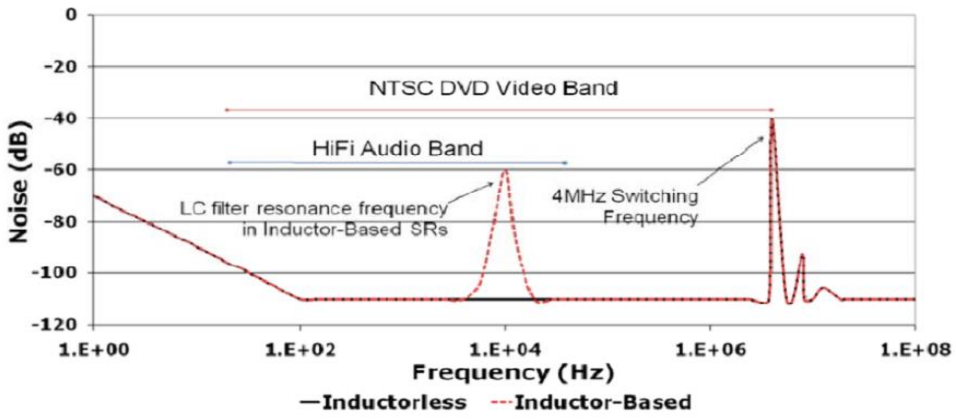


Figure 2-3: Output noise profile of an inductive and switched-capacitor converter [17].

2.3 SCC's Structure and Topology

2.3.1 Structure of SCC

In general, a SCC is comprised of array of switches and array of capacitors. The capacitors are called "flying capacitors". By controlling the switching arrangement of the flying capacitors, the desired output voltage can be obtained. The switching network enables parallel or series arrangement of the flying capacitors during alternative periods. Each switch is turned-on during one or more phases and turned-off in the other phases. The switching period of the switches network is determined by the clock frequency. Each switching period is divided into two or more non-overlapping phases. These phases are denoted Φ_1, Φ_2, and so on. Fig. 2-4 shows one of the basic SCCs with the turn-on phase of each switch is indicated beside the switch.

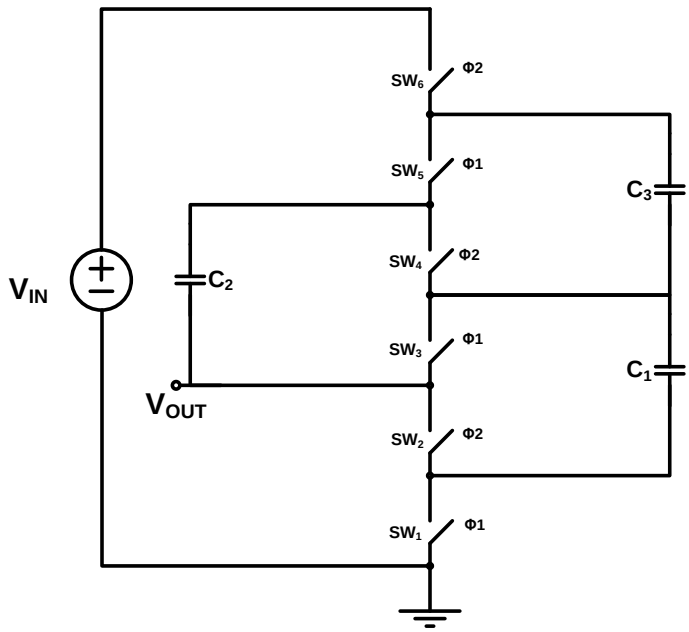


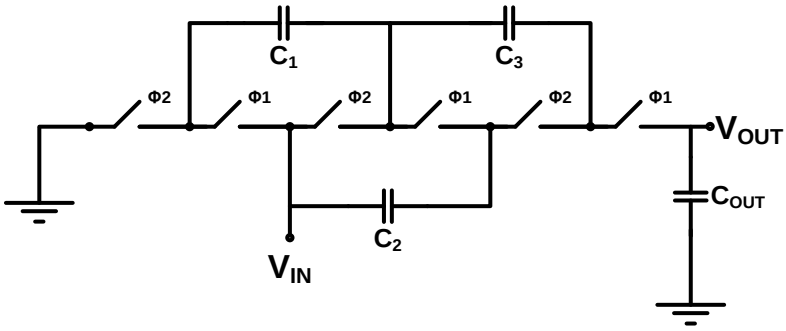
Figure 2-4: Basic switched-capacitor converter with the turn-on phase of each switch indicated.

2.3.2 Review of Existing Topologies

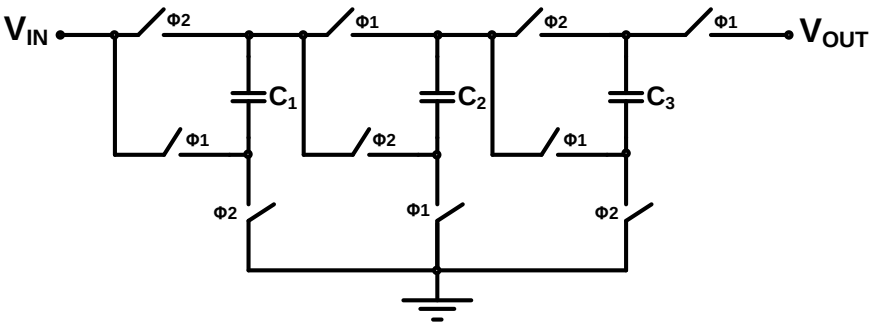
A lot of SCC's topologies have been discussed in several literatures [18-21], such as Dickson, Ladder, Fibonacci, Series-Parallel, and Voltage doubler topologies. Each topology contains a number of capacitors and switches. For the same conversion ratio, the same number of capacitors can be used in the five topologies. The main difference between these topologies is the number of switches that can be used. Selecting between these topologies depend on several conditions such as application, cost, size, performance and so on.

Fig. 2-5 shows the step-down version of the three SCC topologies. It clear from the figure that all the topologies operate between two phases and each switch is turned-on at one phase and is turned-off at the other phase. It can be seen that all the topologies are composed of a basic cell which is a SC voltage divider. Cascading multistage of the basic cell produce a higher conversion ratios but also adds for the SCC complexity.

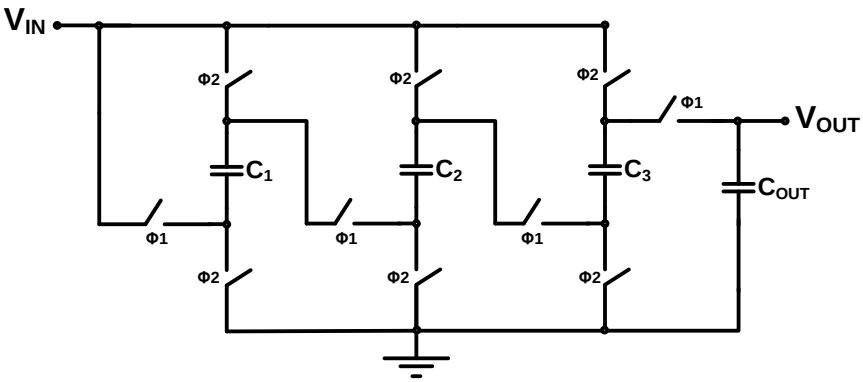
Sometimes, and for regulation purpose, a multiple-gain SCC topology is required. In such topology, the SCC can be configured to obtain different gains depending on adaptive configuration for the topology or external configuration by the user. The multiple-gain SCC is available commercially in the form of integrated circuit (IC). Fig. 2-6 shows some examples for a commercial SCC with a gain of 1/2, 2/3, and 3/4.



(a) Switched-capacitor ladder topology.

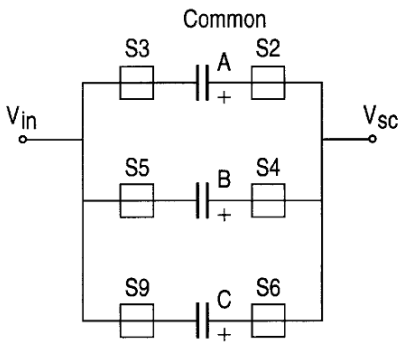


(b) Switched-capacitor Fibonacci topology.

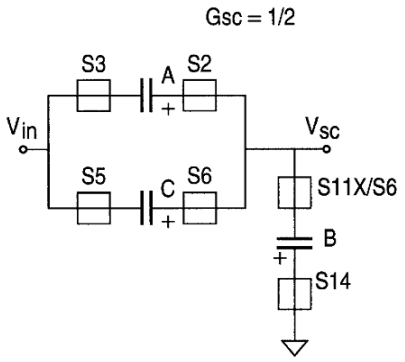


(c) Switched-capacitor Fibonacci topology.

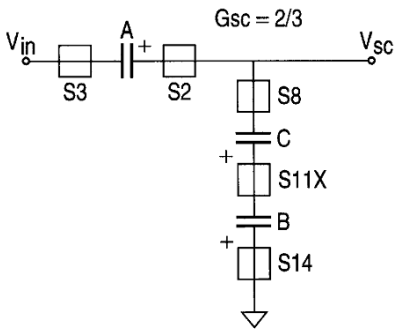
Figure 2-5: Three common topologies for switched-capacitor converters.



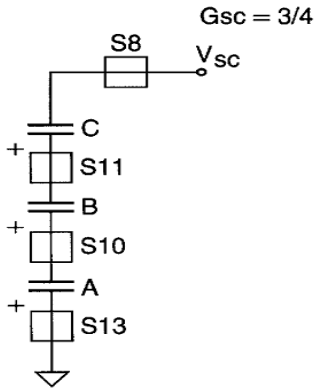
(a) Common phase.



(b) 1/2 gain phase.



(c) 2/3 gain phase.



(d) 3/4 gain phase.

Figure 2-6: The common and gain phases of LM3552 [22].

2.3.3 Topology Selection

A lot of researchers worked on developing SCC topologies that can be reconfigured. Reconfigurable topologies are useful in obtaining various conversion ratios, but also they require large number of capacitors and switches that can be configured at different modes. Most of the time, the capacitors used in these SCC topologies are off-chip capacitors which add for the cost and the size of these solutions. Adding for this, the large number of switches adds more parasitic for the SCC which decreases its efficiency especially at heavy load currents. To ease the design of our SCC, we choose the conversion ratio to be 0.5. So, we choose the simplest topology for voltage divider which is called H-bridge topology. The circuit shown in Fig. 2-7 is for SC voltage divider.

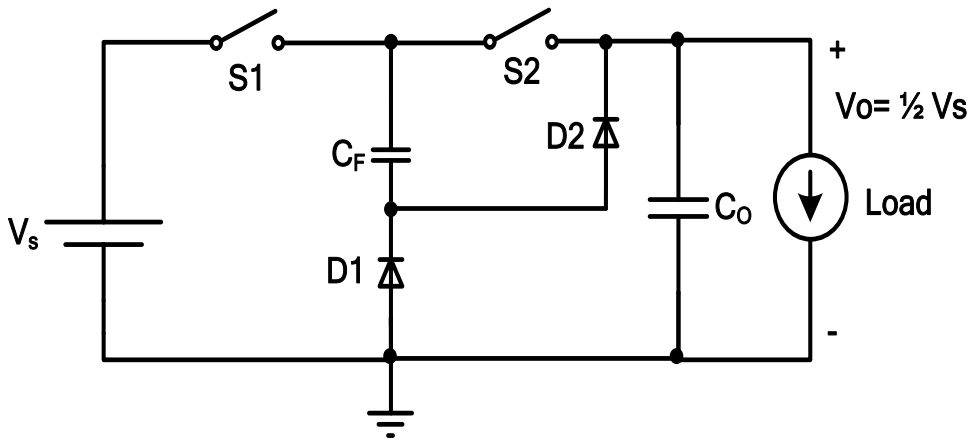


Figure 2-7: SC voltage divider [12].

The SCC topology in Fig. 2-7 is one of conventional topologies. The output capacitor of an SCC is charged and discharged through the switches, so the output voltage is dependent on the switch impedances. In addition, this converter does not regulate output voltage satisfactorily, because

the output voltage cannot be regulated by changing the duty ratio of each switch [12]. The duty cycle is fixed to 50%, thus its output voltage will be affected by input voltage, load current, and internal resistance of the converter.

There is no worry from producing unregulated output from SCC because the second stage, which is buck converter, is already performing the regulation task. For integration, the diodes in Fig. 2-7 are removed and replaced by ideal switches. The new circuit diagram is shown in Fig. 2-8.

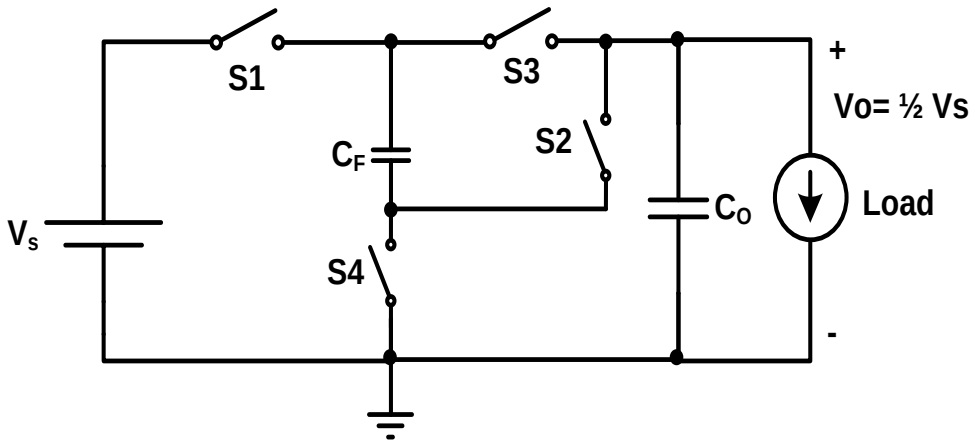


Figure 2-8: Schematic diagram of the H-bridge SCC.

In this topology, we have two capacitors C_F and C_o. Capacitor C_F is called the flying capacitor. The switching network enables series or parallel arrangement of the two capacitors to obtain the required conversion ratio [23]. The operation of the circuit can be divided into two phases. During the first phase, the flying capacitor C_F is connected in series with the input voltage and the capacitor C_o. This phase is called the charging phase and during this phase, the two capacitors charge from the input source. The capacitors configuration during charge phase is shown in Fig. 2-9.

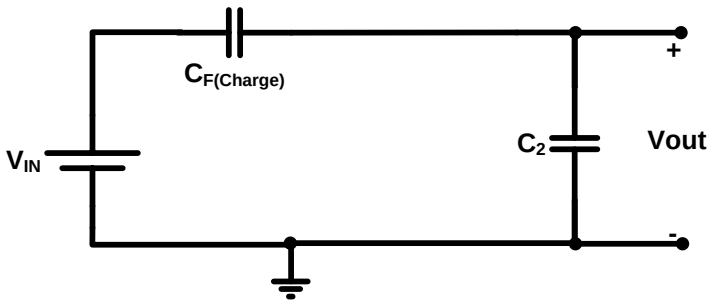


Figure 2-9: Schematic diagram of the H-bridge SCC during charge phase [23].

scharging phase and the load is supplied by the required current through this phasAt the second phase, the flying capacitor C_F is connected in parallel with the output capacitor C_o. This phase is called the die. The capacitors configuration during discharge phase is shown in Fig. 2-10.

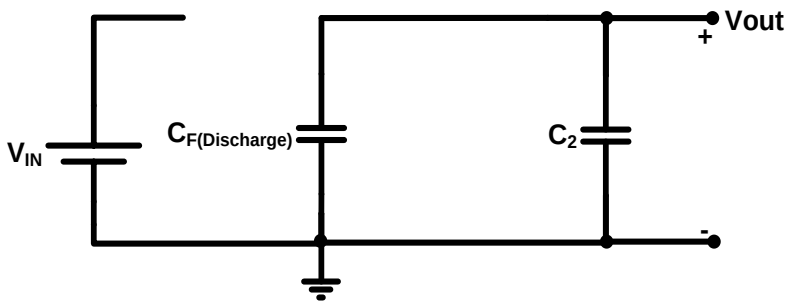


Figure 2-10: Schematic diagram of the H-bridge SCC during discharge phase [23].

In Fig. 2-8 during charge phase, series connection of the flying capacitors is reached by closing the switches S1, S2 and opening switches S3, S4. During discharge phase, parallel connection is reached by closing switches S3, S4 and opening switches S1, S2.

2.3.4 Modeling of SCC

Usually, the output of SCC is unregulated. As mentioned in the previous section, the output of our SCC will be left without regulation. For this reason, the SCC's output will be affected by load and input voltage variations. Our SCC topology roughly divide the input voltage by two and whatever the input voltage value, the output voltage will be approximately half of the input voltage. At fixed input voltage, the output voltage value will depend on the output current (load value).

Regularly, SCC is modeled as shown in Fig. 2-11. The model of SCC consists of ideal transformer with turn's ratio equal to the converter ideal conversion ratio and series output resistance.

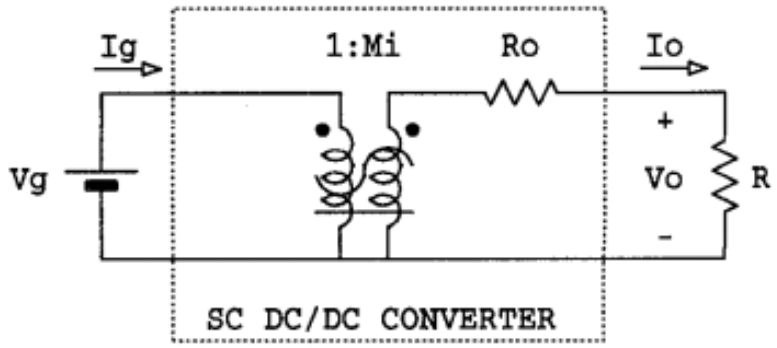


Figure 2-11: SCC DC model [24].

If we assumed that the switches are ideal and the capacitors have no ESR, the series output resistance can be given as:

$$R_O = \frac{1}{fC_F} \qquad (2\text{-}1)$$

In addition to the dependence on the switching frequency and the flying capacitor, the series resistance R_o in the model includes the non-ideal effects like switches' resistance and capacitors' ESR.

Obviously, the equivalent resistance R_o can be minimized by increasing the switching frequency which minimizes the power loss due to this resistance. In addition, the average output voltage is affected by the series resistance because the converter is unregulated. If the value of equivalent series resistance is high, the drop in output voltage may be large under high loading conditions.

2.4 CMOS Realization of Selected SCC

To allow the integration of the SCC circuit, the switches S1, S2, S3, and S4 in Fig. 2-8 are implemented using a 0.25μm CMOS technology. It has been described that S1 and S2 are turned-on and off at the same time. The same is true for switches S3 and S4.

The CMOS technology used is a simple N-well process. This mean that the NMOS transistor is created directly on the P-type substrate and the PMOS transistor is created in the N-well which is built-in into the P-type substrate. This implies that all the NMOS transistors are created in the same substrate which means that implicitly their body is the same. If we tried to implement a power NMOS transistor that its source-terminal is not connected to ground, this will initiate the body-effect because the source-terminal has different potential than the body-terminal (i.e. the P-type substrate). So, we cannot

implement a power NMOS transistor if its source-terminal is not connected to ground.

In Fig. 2-8, only S_4 has a path to ground. This means that we can implement it as NMOS power transistor with its body and source terminals connected together and tied to ground. The switches S_1, S_2 and S_3 have no path to the ground which means that we cannot implement them as NMOS transistors without facing the body-effect problem. So, they are implemented as PMOS power transistors. Fig. 2-12 shows the SCC after implementing the switches in CMOS technology.

The switches M_{P1} and M_{P2} should be turned on or off at the same time, but their gates cannot have the same gate-drive signal as their source terminals have different potentials. At the same manner, switches M_{P3} and M_{N1} should be on or off at the same time but they are different in type which require two different gate-drive signals to drive them. The design of gate-drive circuits will be discussed later.

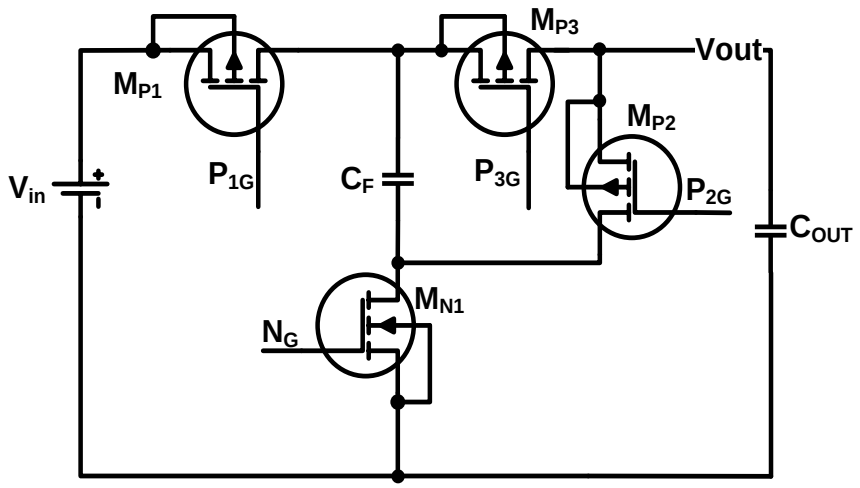


Figure 2-12: SCC power-stage realization using practical CMOS switches

2.5 Power Losses in SCC

The ideal conversion ratio for the H-bridge SCC is 1/2. This ideal conversion ratio is applicable only if all switches are ideal with no internal resistance and the capacitors' ESR can be neglected. Practically this is not true. The ideal conversion ratio is valid only at no-load conditions. However, under different loading conditions this conversion ratio will not be applicable due to power loss in the converter. The power loss of SCC can be classified mainly into two categories; conduction loss and switching loss.

2.5.1 Load Dependent Losses

Current flow through non-ideal power transistors, filter elements, and interconnections results dissipation in each component. Load dependent losses are also called "*conduction losses*" because it depends on the output current.

The load dependent conduction losses can be classified as follows [25]:

- Transistor "ON" resistance losses.
- ESR of flying capacitors.
- Wirebonds and traces resistances losses.

The SCC model in Fig. 2-11 is useful in explaining the conduction power loss. The series output resistance R_O as predicted by Eq. 2-1 is depending on switching frequency in addition to the value of flying capacitor. However, conduction power loss not only depends on these factors. Any parasitic

resistances in the path of the average output current I_O will produce a conduction power loss. The layout metallization, wire-bonding, and packaging parasitic resistances will have a significant effect on the conduction loss and should be taken into account.

Fig. 2-13 shows the SCC power-stage after adding the packaging and wire-bonding parasitic.

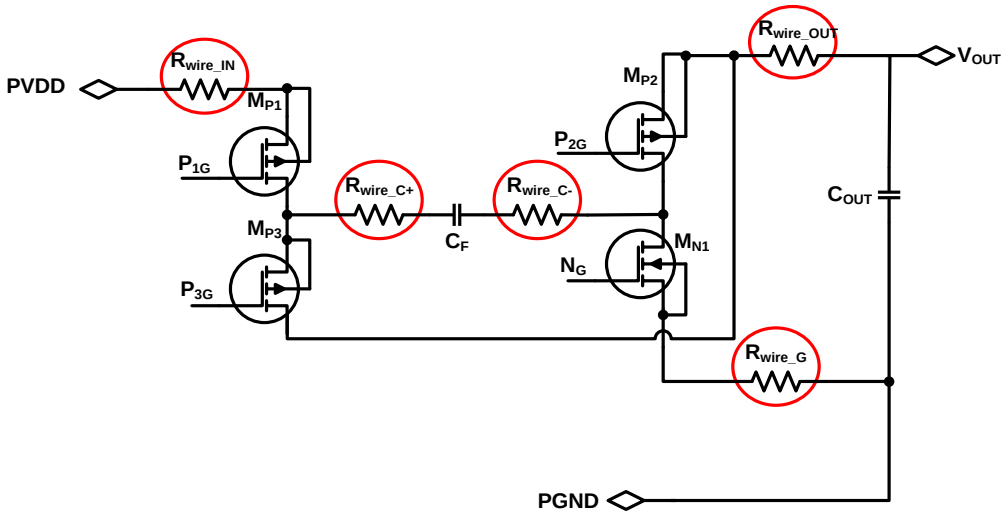


Figure 2-13: SCC power-stage after adding expected parasitic resistances

where:

R_{wire_IN}: *the wrie-bond resistance of input pin.*

R_{wire_OUT}: *the wrie-bond resistance of output pin.*

R_{wire_G}: *the wrie-bond resistance of ground pin.*

R_{wire_C+}: *the wrie-bond resistance of capacitor first terminal pin.*

R_{wire_C-}: *the wrie-bond resistance of capacitor Second terminal pin.*

It is noted from Fig. 2-13 that there are some resistances that will be involved during all the operation phases and some resistances will appear during only one phase. For example, R_{wire_C+}, R_{wire_C-}, and R_{wire_OUT} will appear during the two phases of operation. R_{wire_IN} will appear in the charging phase only and R_{wire_G} will appear in the discharging phase only. In addition for the wire-bonding resistances, layout metallization will add more resistances for the source and drain terminals of any switch. These metallization resistances will also add for the conduction loss.

For a given average output current I_O, the conduction loss P_C can be found as:

$$P_C = {I_O}^2 . R_O \qquad (2\text{-}2)$$

As stated in (2-2), the conduction loss is strongly depending on the series output resistance of the converter R_O. Off course R_O can be decreased if the following considerations taken into account:

- Increase the SCC switching frequency. This is a conclusion from (2-1).
- Choose a flying capacitor with low ESR.
- Decrease the wire-bonding resistance.
- Decrease the MOSFET switches on-resistance as we can.

Increasing the SCC switching frequency will help in minimizing the converter resistance and decreasing conduction loss. Unfortunately,

increasing the switching frequency decreases the conduction loss but add for the switching loss as will be discussed.

The second approach is already reached by choosing ceramic-type capacitors. Ceramic capacitors have low ESR value over a wide range of frequencies which suits our application.

The third approach of decreasing wire-bonding resistance can be obtained by using many wires as possible as we can for each pin in the converter. Using shorter and wider cross-section wires will also decrease the wire-bonding resistance.

The last approach is the most important one because switches on-resistance is the most significant source for conduction loss.

The on-resistance of any MOSFET switch R_{DSON} can be given by the following equation:

$$R_{DSON} = \frac{1}{\lambda . K . \frac{W}{L} \, (V_{GS} - V_{th})^2} \qquad (2\text{-}3)$$

Where λ is the channel-length modulation parameter and K is the trans-conductance parameter and defined as:

$$K = \mu \, . \, C_{ox} = \mu \, . \frac{\varepsilon_{ox}}{t_{ox}} \qquad (2\text{-}4)$$

Where (μ) is the mobility of electron/hole if the MOSFET is N-type/P-type. It is clear from (2-3) that the on-resistance of any MOSFET is inversely proportional to (W/L). In order to decrease the MOSFETs R_{DSON}, one can use MOSFETs with very large widths. This will momentarily minimize the conduction loss, but will also increase by the same factor the parasitic capacitances of the MOSFETs which have a big effect on the switching loss.

2.5.2 Switching Frequency Dependent Losses

As the MOSFET switches on and off, its intrinsic parasitic capacitance stores and then dissipates energy during each switching transition. The losses are proportional to the switching frequency and the values of the parasitic capacitances [26]. This type of loss is also directly called "*switching loss*".

Switching loss is composed of several parts: MOSFET switching loss, MOSFET gate drive loss, and body-diode loss.

I. MOSFET Switching Loss

It is a natural result of charging the parasitic capacitances present at each node in the circuit with a continuous toggling voltage. The toggling rate of this voltage is the clock frequency or switching frequency of the converter. Mainly, the switching loss can be given as the summation of all parasitic capacitances losses which given by:

$$P_{sw} = \sum_{i=1}^{n} C_i \, V_i^{\,2} \, f_s \qquad (2\text{-}5)$$

where:

C_i: *the parasitic capacitance at the* i^{th} *node in the converter circuit.*

V_i: *the voltage across this capacitance.*

f_s: *the converter switching frequency.*

n: the number of parasitic capacitance in the converter circuit.

From (2-5), it can be stated that the effect of switching frequency on the MOSFETs switching loss will be the opposite of its effect on the conduction loss. As the switching frequency increases, the MOSFETs switching loss will increase by the same factor.

II. Gate Drive Losses

The gate drive loss is the power consumed during charging and discharging the gates' capacitances of power MOSFETs. This power is provided by the gate drive circuit and lost between the charging and discharging processes. Gate-drive loss is independent of load current and will therefore degrade light load efficiency [27]. The gate drive loss for a MOSFET can be given as following [28]:

$$P_{GD} = Q_g . V_{Driver} . F_{SW} \qquad (2\text{-}6)$$

where:

Q_g : *the total gate charge of the MOSFET.*

V_{Driver}: *the gate driver power supply voltage.*

F_{SW}: *the switching frequency.*

The gate drive loss can be minimized by managing the amount of charge supplied for the MOSFET. Sometimes, we supply the MOSFET gate capacitances by a large amount of charge that exceeds what it need to turn-on or turn-off. If we managed the amount of charge supplied by the gate drive circuit, we could save a significant part of the gate drive wasted power. The supplied charges are depending on the drivers' size. This means that large-size gate drivers supply high current and waste large amount of charge.

2.5.3 Static Power Loss

Sometimes, this type of power loss is called "*Quiescent Power Loss*". From its name, this power is independent on neither frequency nor load and always has a fixed value. This power loss comes from the quiescent current that is required to operate the controller circuits. Normally, this quiescent current comes from a low voltage supply that is design in the system to supply the controller circuits.

The quiescent power loss is low compared to the other losses in the converter. But its effect becomes significant at light loads. There is no way

to reduce its effect at light load especially if PWM operation is still employed at light loads. One common solution for this problem is to operate the system at pulse frequency modulation (PFM) mode at light loads. This would help in decreasing the switching loss as the switching frequency will not be fixed. In addition, the most power consuming circuits in the controller can be turned-off as PFM operation requires fewer circuits.

2.6 Design of High Efficiency SCC

In this section, the main parts of integrated SCC will be designed using a CMOS technology. Figure 2-14 shows the parts which will be designed through this section. The design procedure of SCC's power-stage includes the optimization of capacitors size, power switches size, and efficiency optimization. The controller design will be discussed at the end of the chapter.

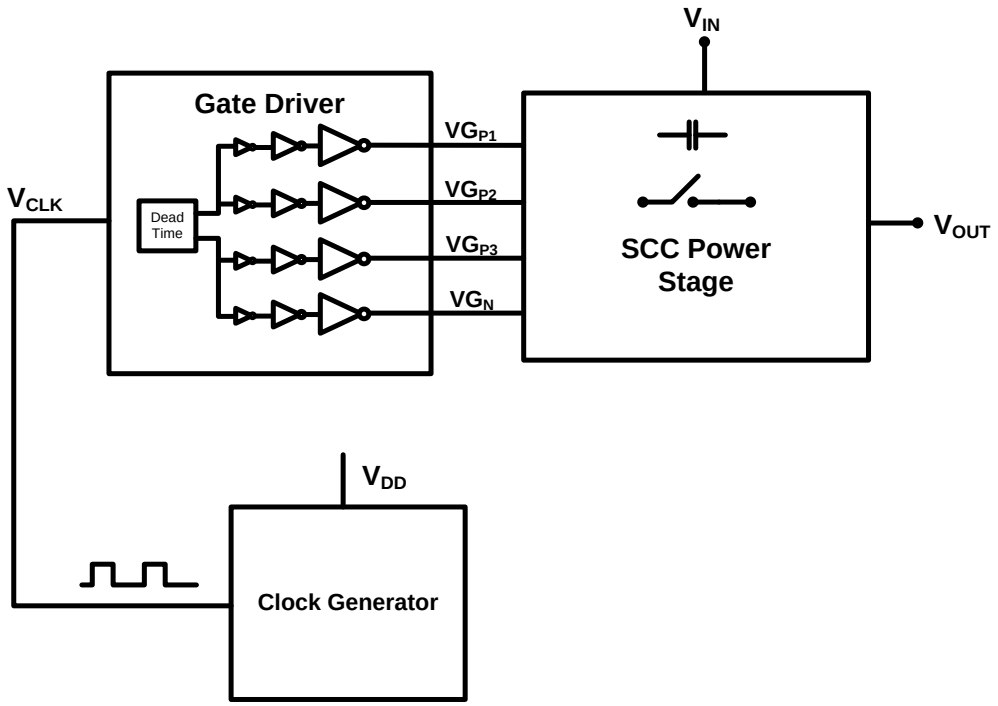


Figure 2-14: Block diagram of SCC sub-blocks.

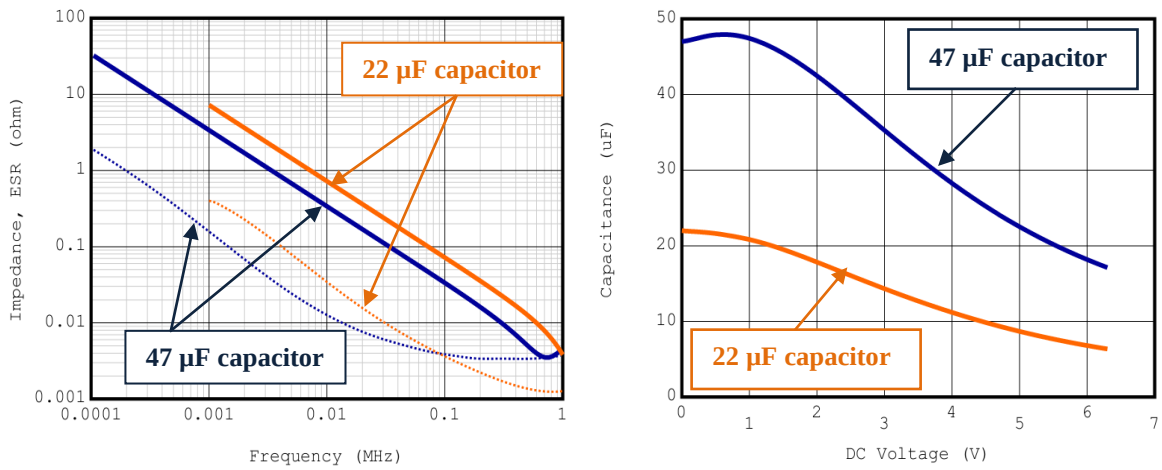
The converter is optimized to convert a 6 V into 3 V with 2 A nominal output current and 3.5 A maximum output current. The converter is designed using 0.25 µm CMOS technology using LV devices.

2.7 Power Stage Design

2.7.1 Capacitors selection

The flying capacitor is responsible for maintaining and transferring the energy from the input to output. The output capacitor has the role for minimizing the output voltage ripple and equally sharing the input voltage with the flying capacitor. The selection of the capacitor sizes is directly relying on the switching frequency of the converter. It can be noted from (2-1) that the ideal SCC has an equivalent series resistance that is inversely proportional to the switching frequency and flying capacitor value.

Ceramic capacitors are well suited to SCC due to their small size, high energy density, low ESR, low cost, and wide availability. Also, their value is not degraded very much with temperature and frequency variations. For the flying capacitor C_F, a configuration of two parallel capacitors is selected. The configuration consists of a 47 µF 1206 capacitor in parallel with a 22 µF 0805 capacitor. This configuration is selected to minimize the ESR value of the configuration and help in minimizing the equivalent series resistance of the SCC. The ESR, impedance, and capacitance variation due to the applied DC voltages for the capacitors is shown in Fig. 2-15.



(a) Z and ESR of 47µF and 22µF capacitors.

(b) Capacitance vs. DC biasing of 47µF and 22µF capacitors.

Figure 2-15: The selected capacitors electrical characteristics [29].

2.7.2 Optimum Switching Frequency Selection

The converter switching frequency controls the value of series equivalent resistance R_O and the output voltage ripple. Higher switching frequency leads to lower R_O, lower ripple, and smaller capacitor size. Current trend of power converters is very high switching frequency due to its advantage in minimizing the size of bulky components such as capacitors. However the switching frequency become very critical if the converter efficiency is the most important target for the system. Losses increase dramatically with the increase of switching frequency which decreases the system efficiency. For high current converters, the efficiency target cannot be reached easily by decreasing the switching frequency. Decreasing the switching frequency at such converters minimizes the switching losses but the conduction losses will dominate the total loss in the converter.

It is complicated to calculate the optimum frequency at which the conduction and switching losses are equal. To select the optimum switching frequency, a scan for the resulted efficiency is applied at a random three frequencies to help us in predicting the best switching frequency. The plot of efficiency versus output current at 100 KHz, 200 KHz, and 500 KHz is shown in Fig. 2-16 for VIN=6V and MOSFETs widths of 160 mm.

The efficiency plot shows that the optimum switching frequency is 200 kHz (between 100 kHz and 500 kHz).

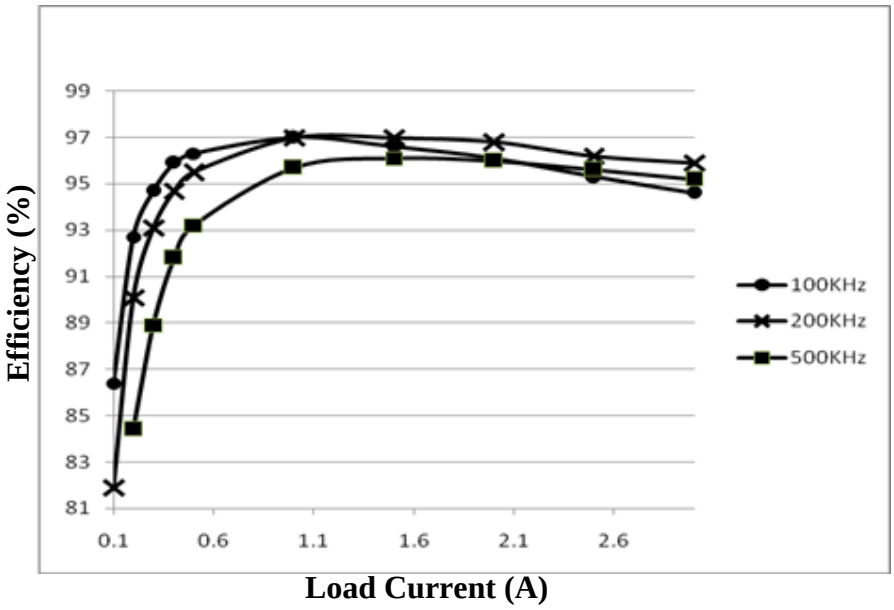


Figure 2-16: Efficiency vs. output current at different switching frequencies

2.7.3 Power MOSFETs Design

The design of power MOSFETs used for implementing the converter switches can be done by designing the width of each MOSFET switch. According to Eq. 2-3, the switch on-resistance is inversely proportional to the MOSFET width. By contrast, the parasitic capacitance of a MOSFET is directly proportional to the MOSFET width.

There is a trade-off between the on-resistance and parasitic capacitance of a MOSFET. Minimum conduction loss requires minimum on-resistance which can be reached using very wide MOSFET. On the other hand, minimum switching loss requires minimum parasitic capacitances which can be reached using the least width for MOSFET. The conduction loss and switching loss are opposite to each other. To get maximum efficiency from a converter, an optimum width for the MOSFET should be selected. At this width, the conduction loss and switching loss can reach a minimum value at a specific output current and specific switching frequency.

In order to select the optimum width for our converter MOSFETs, we should fix all other parameters that affect the converter efficiency such as input voltage, output voltage, output current, and switching frequency. The switching frequency is previously selected and its value has been fixed to 200 kHz.

The SCC has four power MOSFETs. Three of these MOSFETs are PMOS-type and one is NMOS-type. It is known that for the same technology NMOS MOSFET has lower on-resistance than PMOS MOSFET by a ratio ranges from 2.5 to 3 times. For matching the switches resistance during charging and discharging phase, the width of PMOS MOSFETs should be

2.5 higher than NMOS MOSFET. Fig. 2-17 shows the efficiency versus power MOSFET's widths at an output current value of 2A which approach half of the converter maximum output current capability.

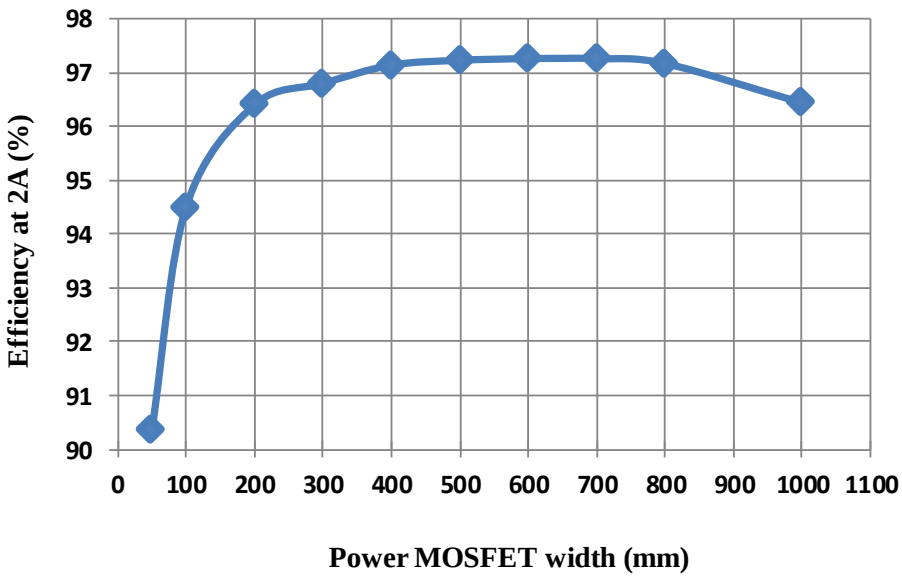


Figure 2-17: Efficiency vs. power MOSFET width at 2A load and 200 KHz frequency.

It is noted from Fig. 2-18 that the maximum efficiency is obtained at MOSFET's width of 400 mm. This width belongs to any power PMOS MOSFET in the converter and the power NMOS MOSFET becomes 160 mm. These widths are the optimum values for an output current of 2 A. The converter efficiency will be lower at both high load and light load. At high loads, the efficiency is dominated by the conduction loss which is higher for the designed MOSFET's widths. At light-loads, the efficiency is dominated by the switching loss because the output current become low and the wide width MOSFETs become no longer useful.

2.8 Gate Drive Design

There are numerous models available to illustrate how the MOSFET works; nevertheless finding the right representation might be difficult. A really useful MOSFET model which would describe all important properties of the device from an application point of view would be very complicated [30]. Fig. 2-18 shows the switching model of any power MOSFET. This model includes most of the parasitic parameters that affect switching behavior of a MOSFET.

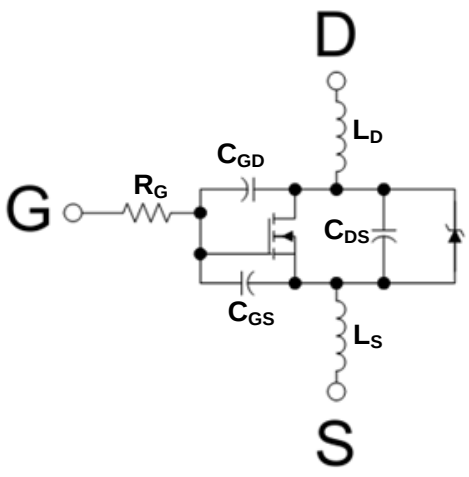


Figure 2-18: Power MOSFET model [30].

In high speed applications, the parasitic capacitances of a MOSFET are the most important parameters that affect its speed. Normally the value of these parasitic capacitors is high for a power MOSFET. They are considered as a capacitive load for the circuit that produces the gate signal for the MOSFET. The gate-driver circuit is used when a clock circuit (gate signal generator) cannot provide the output current required to drive the gate capacitance of the associated MOSFET.

The effectiveness of the gate-driver circuit depends on the ability to source or sink a sufficient current to turn-on or off the MOSFET in a fast way. One of the most popular drive circuits for driving MOSFETs is CMOS totem-pole driver. This driver is shown in Fig. 2-19.

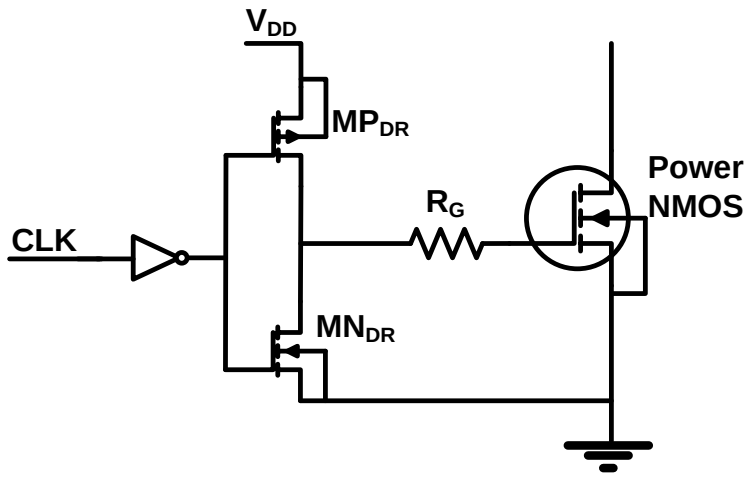


Figure 2-19: Totem-pole driver for NMOS power MOSFET.

It is clear that this totem-pole driver has an inverting property, so it is preceded by a simple inverter. The totem-pole driver can be considered as conventional buffer-stage with relatively large size. The transistor MP_{DR} supply the current required to charge the input capacitance and turn-on the MOSFET. While the transistor MN_{DR} sinks the current required to discharge the input capacitance and turn-off the MOSFET. By careful design for the driver transistors, the amount of current that is used for driving the power MOSFETs can be adjusted.

More effort should be exerted to prevent shoot-through problems. Shoot-through is defined as the condition when both MOSFETs are either fully or partially turned on, providing a path for current to "shoot-through" from the

input voltage to the ground [31]. In our SCC, we have four switches where each two switches turn-on during one phase and turn-off at the second phase. Turning-on two power MOSFETs from different phases can create a current path from input to output, from input to ground, or from output to ground. In order to avoid the shoot-through problems, a dead time should be inserted between the switching signals of each phase. The dead time insertion can be made using a simple break before make circuit. The break before make circuit is shown in Fig. 2-20.

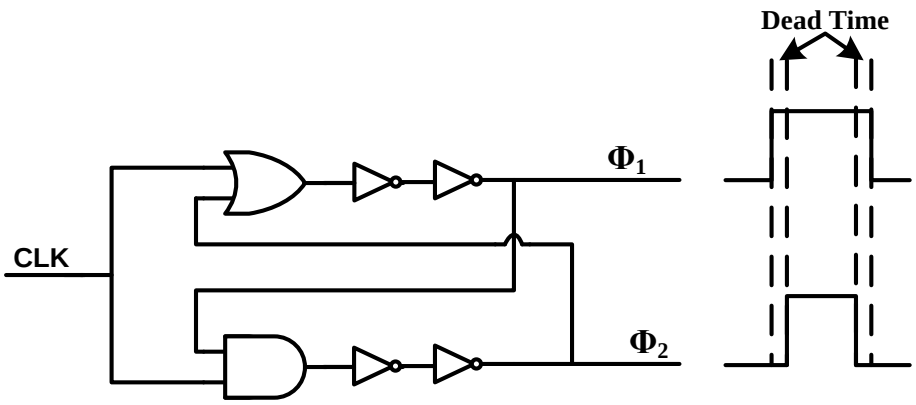


Figure 2-20: Break before make dead time circuit.

In Fig. 2-20, the clock signal is applied for the dead time circuit and then separated into two different signals Φ_1 and Φ_2 where Φ_1 is the control signal for charging phase MOSFETs and Φ_2 is the control signal for discharging phase MOSFETs.

In each phase of operation two power MOSFETs should be turned-on and the other two MOSFETs should be turned-off. However, the gate signals required for MOSFETs in the same phase are different. This can be

understood by looking again at the SCC power stage and its power MOSFETs. Keeping in mind that power MOSFETs are implemented using 0.25 µm CMOS technology. It implies that the maximum voltage swing for V_{gs} of each MOSFET must not exceed 2.5V. Based on this, the driving voltages for each MOSFET is shown in Fig. 2-21.

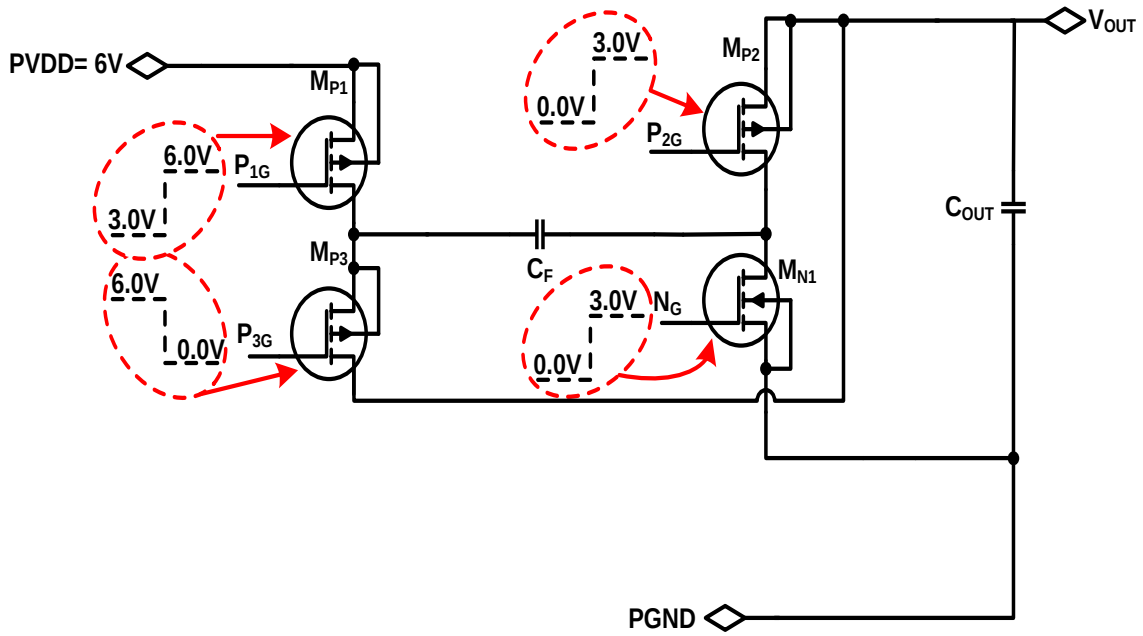


Figure 2-21: SCC power MOSFETs with their driving voltages highlighted

Fig. 2-21 shows that transistor M_{P2} and M_{N1} can be derived directly using the totem-pole driver circuit shown in Fig. 2-19. The situation is different for M_{P1} and M_{P3} which cannot be directly derived from our gate driver circuit. In order to generate the gate signals for these transistors a reduced gate swing circuit is needed. The reduced gate swing circuit is shown in Fig. 2-22.

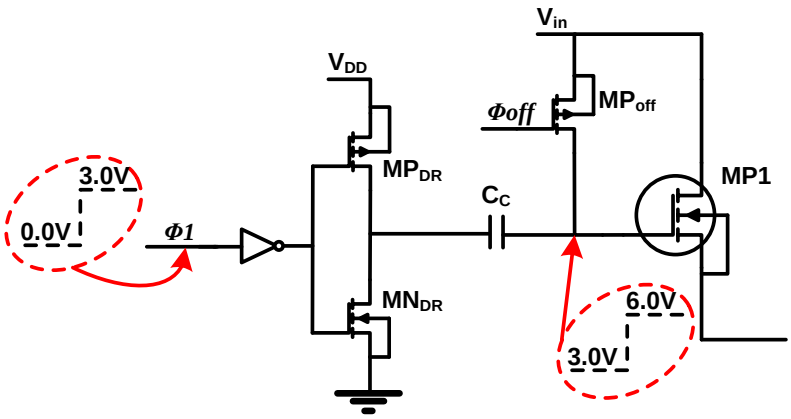


Figure 2-22: Reduced gate swing driver for M_{P1} [26].

However, the reduced gate swing driver can be used for driving M_{P1} only. Power transistor M_{P3} needs a gate swing voltage from 0 V to 6 V. To produce such signal, the driver for M_{P3} should be powered from V_{in}. The reduced gate driver circuit will be used to produce the gate signals for the driver itself. This can be described in Fig. 2-23. The gate drive circuit for all the power MOSFETs in the SCC power stage can be integrated into one circuit which is shown in Fig. 2-24.

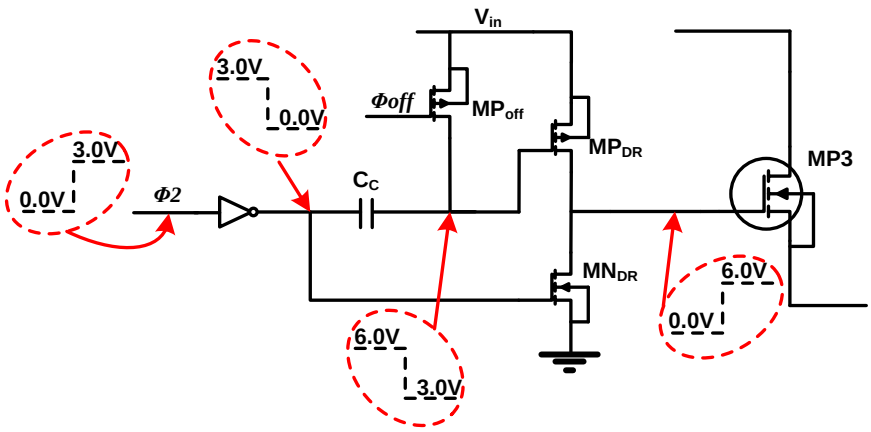


Figure 2-23: Gate driver circuit for M_{P3}.

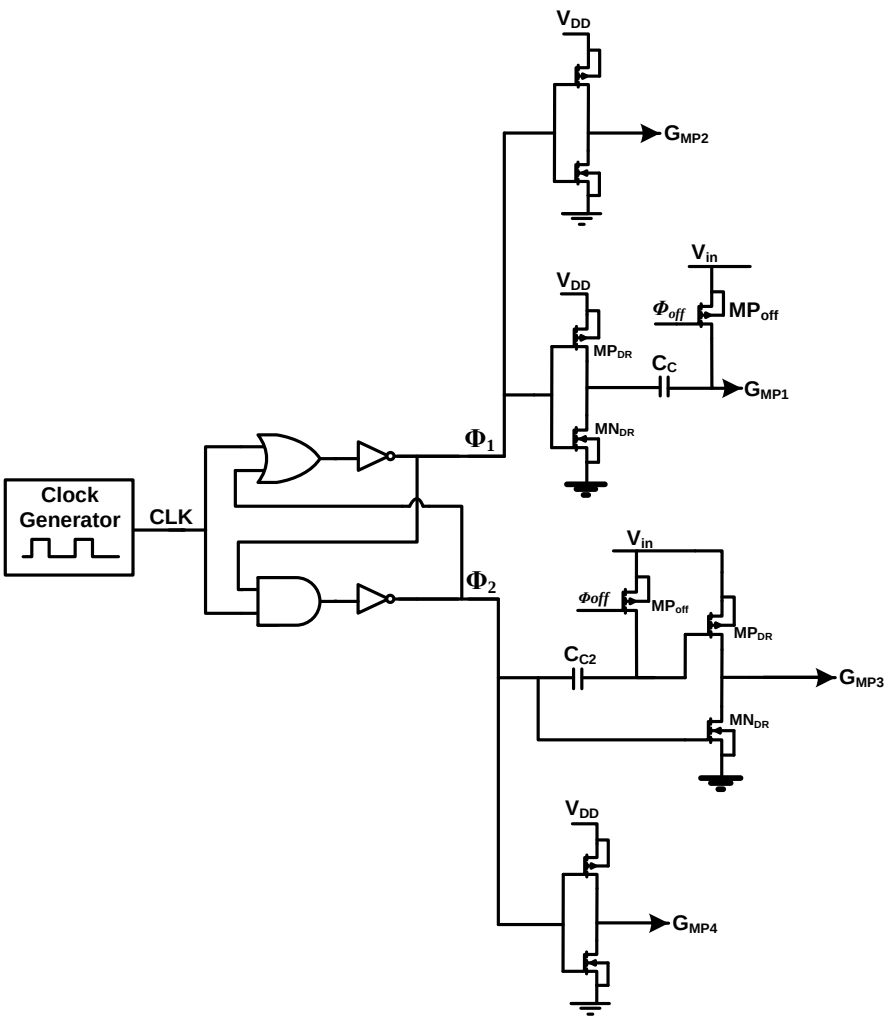


Figure 2-24: Total gate driver circuit for SCC power MOSFETs.

2.9 Clock Generator Design

The clock generator circuit is the circuit that produces the clock signal needed for the switching network of SCC. The clock generator circuit can be realized using CMOS ring oscillator. However, the frequency range of the ring oscillator cannot reach the kHz range as in our case. One possible approach is to design a ring oscillator in the megahertz range and then divide the frequency to obtain the required frequency. Even this approach cannot give an accurate frequency since the propagation delay for each stage in the oscillator cannot be predicted and the oscillator has a relatively poor phase noise response.

The common idea in designing oscillators for DC-DC converters is to charge and discharge a capacitor with a constant current. The capacitor's voltage is compared to a constant voltage levels where the status of comparator's output will be toggled between 0 V and V_{DD}. The clock generator circuit is shown in Fig. 2-25. The operation of the circuit can be explained as following:

- The capacitor C is charged by a constant current I_{CH}. The capacitor's voltage is applied for the comparator to be compared to the voltage across R_1 and R_2.
- When the capacitor voltage reaches a value equal to the voltage across R_1 and R_2, the comparator's output goes high.
- The high status of comparator's output enables the discharging circuit for the capacitor and changes the voltage level applied to the comparator to the voltage across R_2 only.

The resulted clock signal is shown in Fig. 2-26 with a frequency of 200 KHz at room temperature.

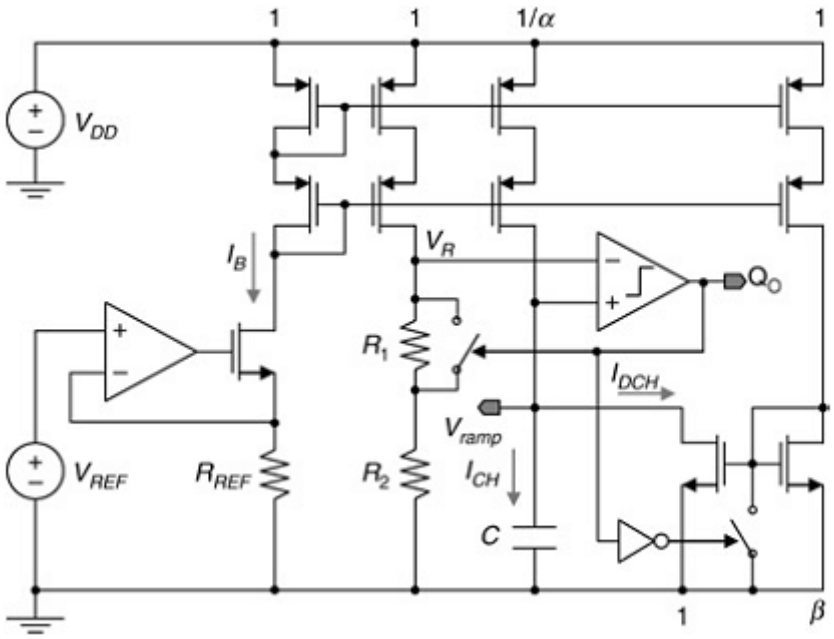


Figure 2-25: Clock generator circuit [32].

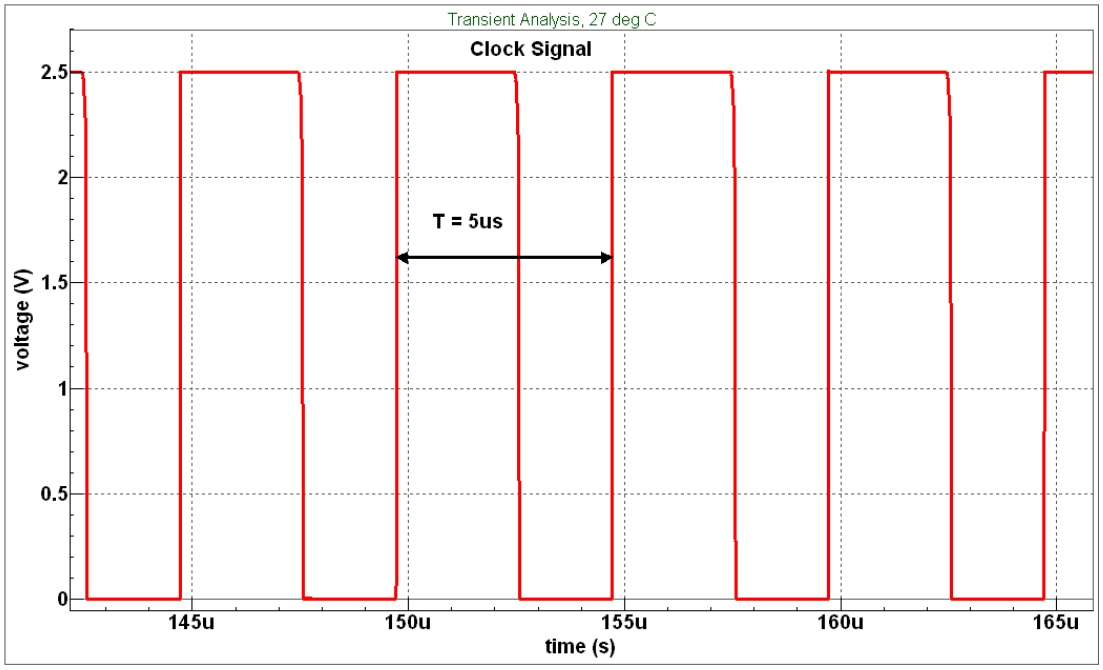


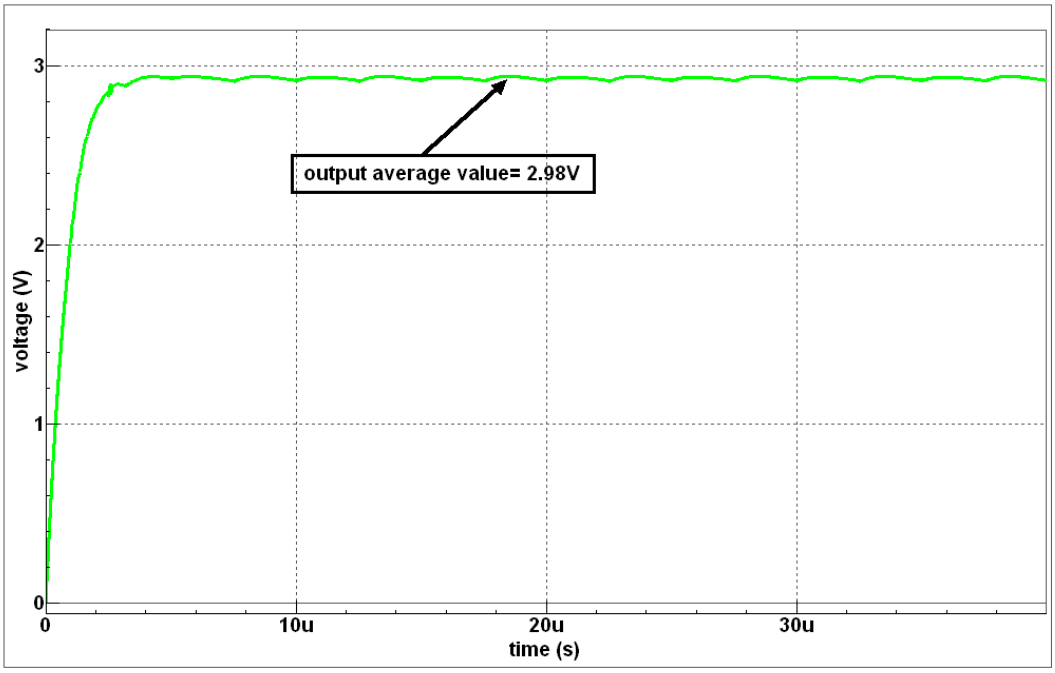
Figure 2-26: Clock signal with 200 KHz frequency.

2.10 SCC Integration and Simulation Result

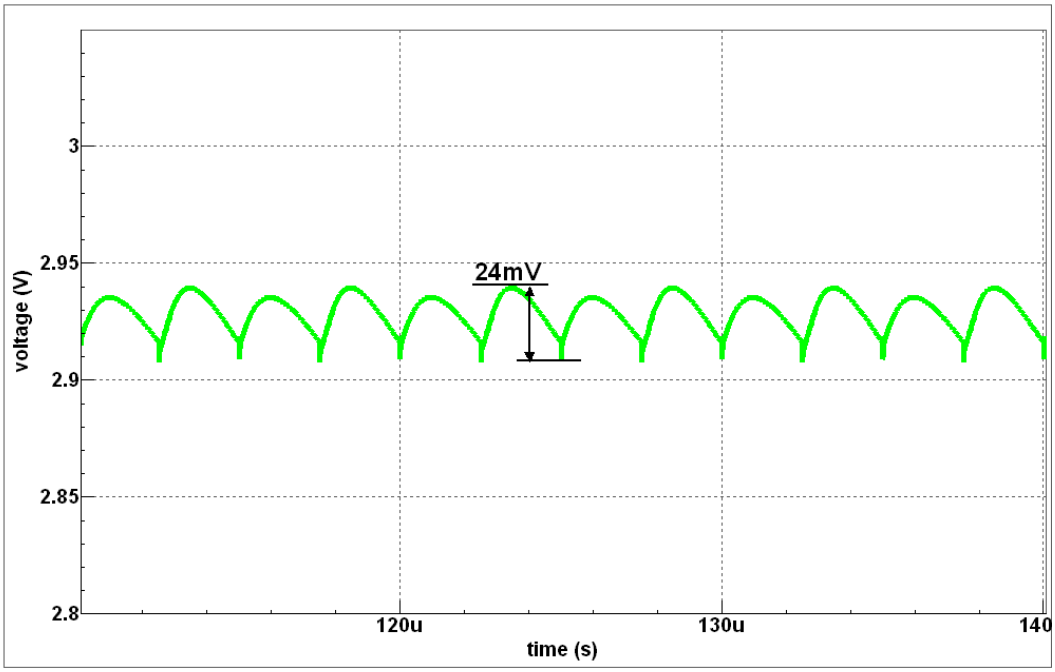
The SCC system indicated in Fig. 2-14 is integrated and simulated using 0.25 µm technology. Fig. 2-27a shows the simulation result for the SCC output voltage at output current 2 A. The figure shows that the average value for the SCC's output voltage is around 2.94 V. Fig. 2-27b shows the peak-to-peak SCC's output voltage with the output ripple indicated on the plot. The SCC's output ripple is 24 mV which equal to 0.8% of the output voltage. The ripple percentage is very small which will be ideal for feeding the buck converter in the two-stage system.

The simulation result for the gate-source voltage of each power MOSFET is shown in Fig. 2-28. Clearly from the figure that M_{P1} and M_{P2} are turned-on during the time that M_{P3} and M_{N1} are turned-off.

Referring to Fig. 2-29, the efficiency of SCC circuit can be known at different loading conditions. The converter is optimized for operation over a wide load current range from 0.1 A to 3.5 A. A maximum efficiency of 97.3% is obtained at a load current of 1.3 A while a minimum efficiency of 95.7% is obtained at the maximum load current 3.5 A.



a) SCC's output voltage result



b) SCC output ripple.

Figure 2-27: SCC output voltage waveforms.

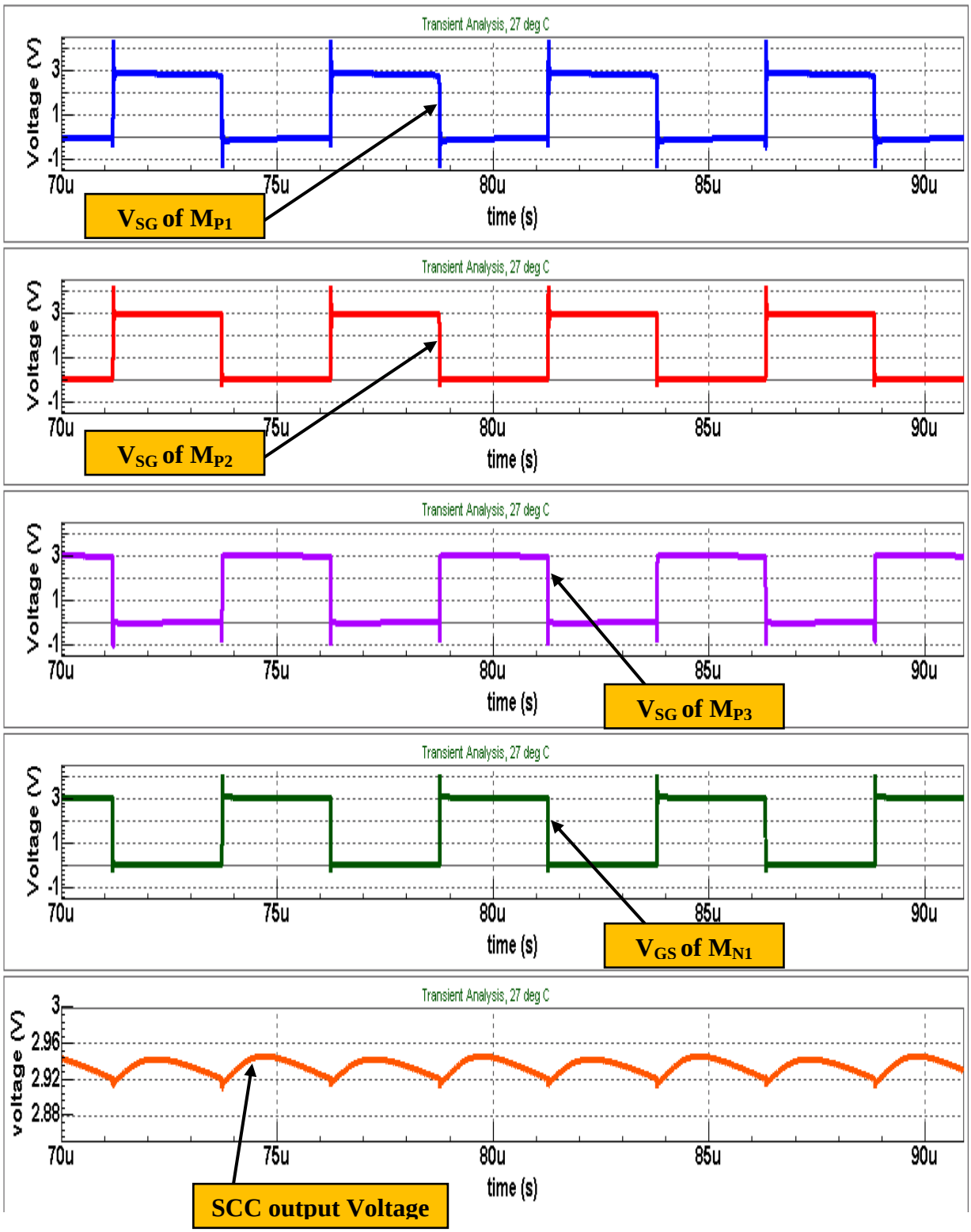


Figure 2-28: The gate-source voltage swing of power MOSFETs.

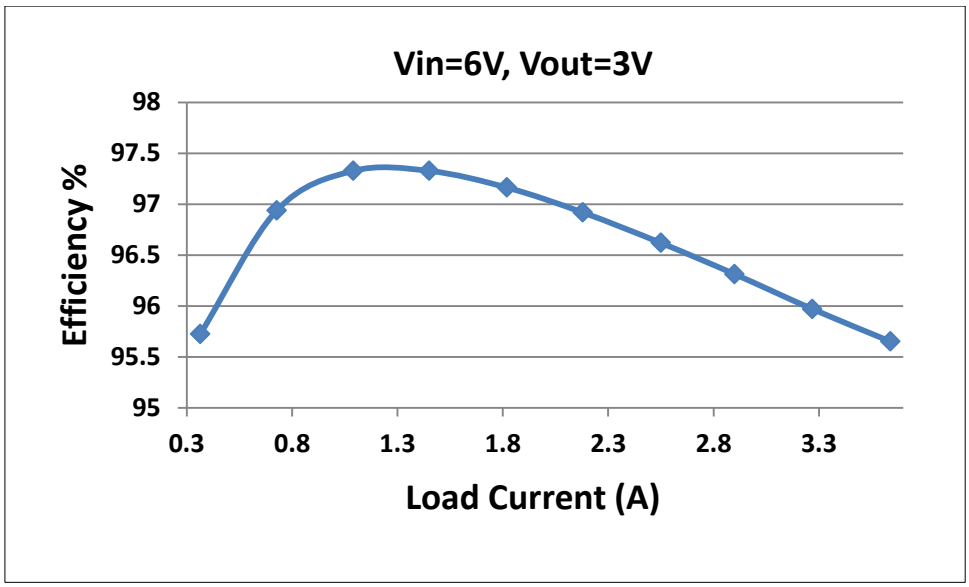


Figure 2-29: The efficiency of the SCC vs. load.

2.11 Conclusion

The analysis and design of a simple step-down switched-capacitor converter has been discussed in this chapter. The converter is targeted to be the first-stage in a two-stage voltage regulator. The SCC has been designed to convert a 6 V to 3 V for a wide load range (0.1 A to 3.5 A). The SCC's output voltage is not regulated because the regulation will be the task of the second-stage. A very high efficiency can be obtained with a maximum efficiency of 97.3% and an average efficiency higher than 96.5% over the predetermined load range. In addition, the CMOS implementation of Power MOSFETs and controller blocks is discussed and realized using a CMOS 0.25 µm technology. Finally, the simulation result for the designed system is provided.

Chapter 3

2 MHz Integrated Buck Converter Design

Chapter 3

2 MHz Integrated Buck Converter Design

3.1 Introduction

For its superior performance, high efficiency, and tight regulation; the buck converter is widely used in the design of high-current low-voltage power supplies for microprocessor applications. More topologies are developed to enhance the performance of conventional buck converter. However, still the conventional buck converter is a brilliant choice for such applications.

In this chapter, the operation theory, analysis and design of buck converter will be discussed in details. A detailed design for every block will be given at the end of the chapter.

3.2 Operation Theory of Buck Converter

From its name "buck", it is a circuit that used to buck or attenuate the input voltage and produce output voltage that is always lower than the input. The buck converter can be simply considered as two ideal switches followed by a simple LC low-pass filter. The first switch connects the input voltage to the low-pass filter and the second switch connects the low-pass filter to ground as shown in Fig. 3-1.

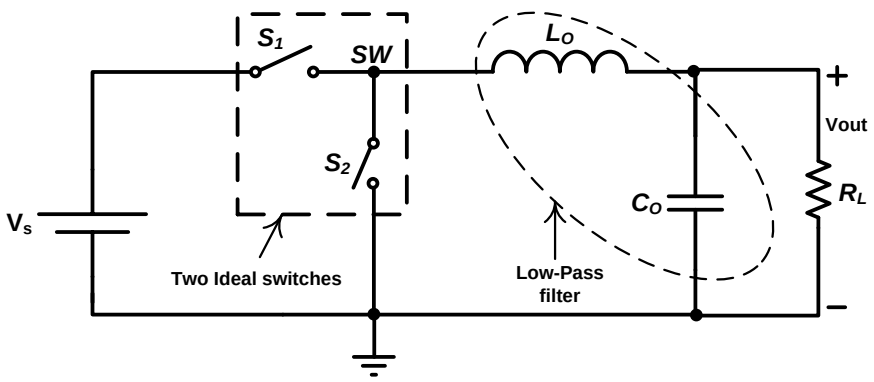


Figure 3-1: Simple representation for buck converter.

In Fig. 3-1, switches S_1 and S_2 together perform as *SPDT* together. The node after the *SPDT* is known as the "*switching node*". Based on the mentioned operation, the voltage at the switching node *SW* voltage can be shown in Fig. 3-2. When S_1 is ON, the voltage at *SW* node will be equal to V_{in}. By the same way, when S_2 is ON, the voltage at *SW* node will be 0. A square-wave shaped signal will be produced by the two switches and then applied to the LC low-pass filter. The low-pass filter is likely to be an average circuit that calculates the average of switching node voltage and apply it on the load as shown in Fig. 3-2.

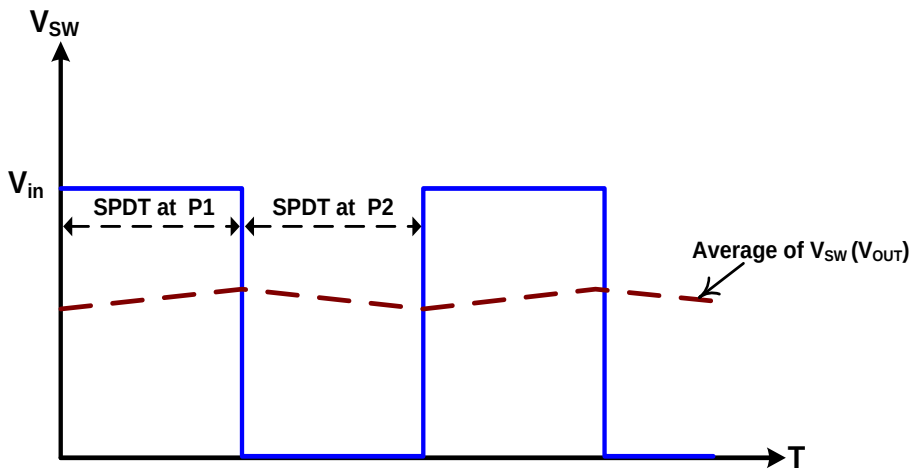


Figure 3-2: Voltage at SW node.

Based on our discussion, it is obvious that the LC low-pass perform likes averaging the switching node *SW* voltage where this average voltage will equal the output voltage of the buck converter. The DC output voltage value depends on the duty ratio of the *SW* node signal. The duty ratio can be identified as the ratio between the time when S_1 is ON and complete switching period and the duty ratio can be given by the following equation:

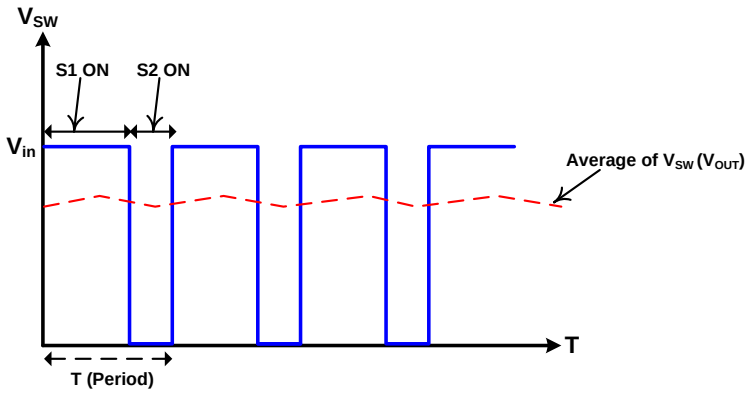
$$D = \frac{T_{S1(ON)}}{T_{S1(ON)} + T_{S1(OFF)}} \tag{3-1}$$

The dependence of buck converter's output on duty ratio can be described as:

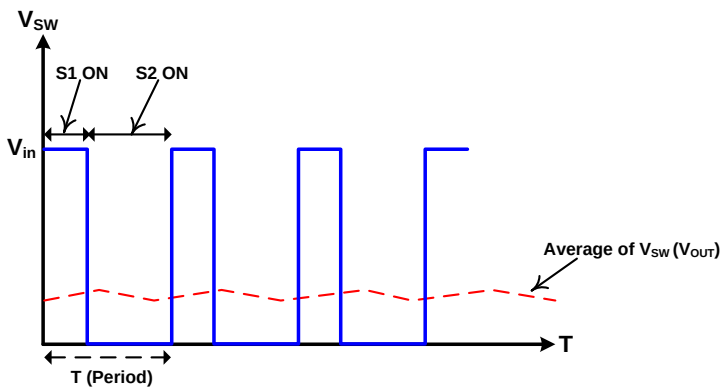
$$V_{OUT} = D.V_{IN} \tag{3-2}$$

Eq. (3-2) states that the average output voltage of a buck converter is a multiplication of the duty ratio of *SW* node voltage and the input voltage V_{IN}.

The higher the duty ratio of *SW* node, the higher the output voltage is. The opposite is true. This can be clarified by Fig. 3-4.



(a) Output voltage at high duty ratio.



(b) Output voltage at low duty ratio.

Figure 3-3: The effect of different duty ratio on the average output voltage.

3.3 Analysis of Buck Converter

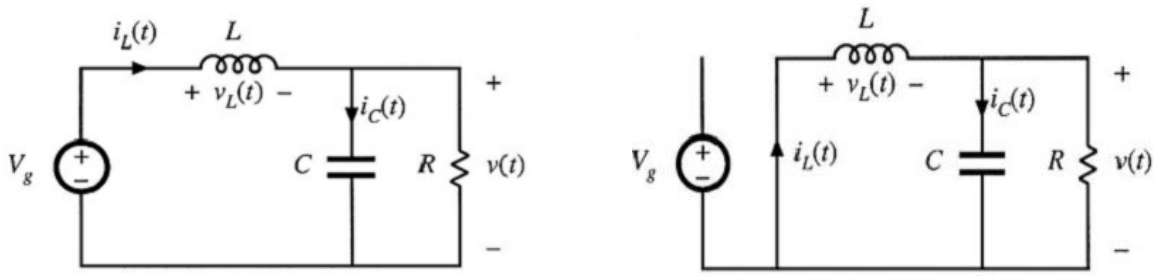
For good understanding for the buck converter, it is important to analyze its ideal circuit that is shown in Fig. 3-1. The analysis of buck converter is made based on the following assumptions:

- The steady-state operation is already reached.
- All the components used are ideal.
- The capacitor value is large enough to maintain constant output voltage.
- The value inductor current never reaches zero.

In Fig. 3-1, we have two switches that are alternately turned-on and off. The alternation is made periodically with a period *T* as followed from Fig. 3-3. However, the average value of output voltage is not affected by the period. Rather than, it is affected by the duty ratio within the period *T*. Thus, the buck converter circuit should be analyzed based on the status of the switches. The switches status can be divided into two cases:

1. When switch S_1 is ON and switch S_2 is OFF.
2. When switch S_1 is OFF and switch S_2 is ON.

These cases are shown in Fig. 3-4.



(a) S_1 is ON and S_2 is OFF. (b) S_1 is OFF and S_2 is ON.

Figure 3-4: Switches ON/OFF cases.

Case 1: Switch S_1 is ON and Switch S_2 is OFF

When switch S_1 is ON and switch S_2 is OFF, the circuit is Fig. 3-4a is applicable. At this case, the input voltage is applied directly for the inductor which enable the charging of the inductor by a current $i_L(t)$. The inductor current ripple during this case can be given by:

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{DT_s} = \frac{V_g - V_O}{L} \qquad (3\text{-}3)$$

where:

Δi_L : *the inductor current ripple (current change during S_1 is ON)*

DT_s: *the time during the switch S_1 is ON.*

V_g: *the buck input voltage.*

V_O: *the average value of output voltage.*

Eq. (3-3) implies that the inductor current changes with time in a slope that is proportional to L and (V_g-V_O). Since V_g is always higher than V_O, bucking property, the slope will always be positive during this case.

From Eq. (3-3), the inductor current ripple during the ON period of switch S_1 can be calculated by:

$$\Delta i_L(S1\ ON) = \left(\frac{V_g - V_O}{L}\right) DT_s \qquad (3\text{-}4)$$

Case 2: Switch S_1 is OFF and Switch S_2 is ON

In this case, the circuit at Fig. 3-4b is applicable. The inductor terminal is connected to ground (zero volts). Because of the stored energy in the inductor, the inductor current continues in flow and completes its path through the ground connection. The inductor current ripple during this case can be given by:

$$\frac{di_L(t)}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1-D)T_s} = \frac{-V_O}{L} \tag{3-5}$$

Again, Eq. (3-5) gives us indication about the behavior of inductor current during case 2. It states that the inductor current changes with time in a slope that depend on (V_O/L) when switch S_2 is ON. It is clear that the slope will be negative which means that the inductor current decreases during this case. Solving for the inductor current ripple from Eq. (3-5) yields:

$$\Delta i_L(S_1\ OFF) = \left(\frac{-V_O}{L}\right)(1-D)T_s \tag{3-6}$$

Eqs. (3-4) and (3-6) give us a clear description for the inductor current during each subinterval. These equations can be used to sketch the inductor current waveform as shown in Fig. 3-6.

It is noted from Fig. 3-5 that the inductor current ripple is symmetrical around a DC component *I*. This component represents the average output current of the buck converter. The inductor current increases by a ripple

magnitude of $\Delta i_{L(S1\ ON)}$ during the first sub-interval (case 1) and then decreases by a ripple magnitude of $\Delta i_{L(S1\ OFF)}$ during the second sub-interval (case 2).

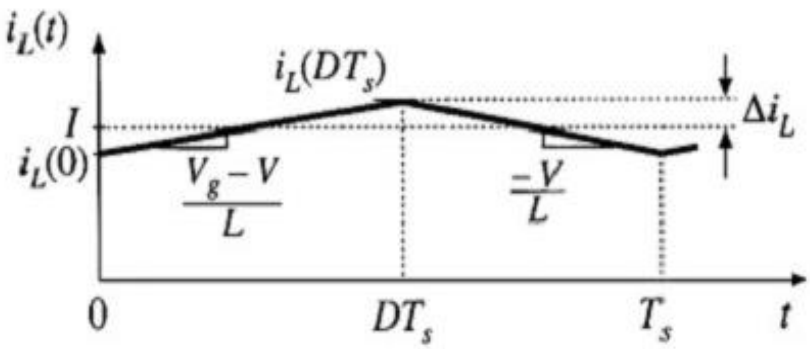


Figure 3-5: Steady-state inductor current waveform [33].

The requirement that, in equilibrium, the net change in inductor current over one switching period be zero leads us to a way to find steady-state conditions in any switching converter [33]. The change in inductor current within a complete switching period can be obtained by adding the change in inductor current during the two subintervals as follow:

$$\Delta i_L(S_1\ ON) + \Delta i_L(S_1\ OFF) = 0 \tag{3-7}$$

Substituting from Eqs. (4-4) and (4-6) into Eq. (4-7) yields:

$$\left(\frac{V_g - V_O}{L}\right) DT_s + \left(\frac{-V_O}{L}\right)(1 - D)T_s = 0 \tag{3-8}$$

Solving the above equation for V_o yields:

$$V_O = D\ V_g \tag{3-9}$$

Eq. (3-9) coincides with Eq. (3-2) that previously mentioned.

3.3.1 Output Ripple Calculation

In DC-DC converters the output voltage ripple is a measure of the deviation in the output voltage from the average value. The peak-to-peak voltage ripple for the buck converter for the continuous conduction mode can be calculated for a specified value of output capacitance by calculating the additional charge ΔQ provided by the ripple current in the inductor. This analysis assumes that the entire ripple current flows through the capacitor, while the average value of the inductor current flows through the load resistor [34]. The output voltage ripple can be approximated by evaluating the capacitor current which can be used to evaluate the capacitor charge. If we have a good estimation for the capacitor charge, the output voltage ripple can be easily evaluated.

Consider the waveform in Fig. 3-6 where the capacitor current is shown within a complete switching period. The change in capacitor voltage can be related to the total charge q contained in the positive portion of the capacitor current waveform [33]. The charge Δq can be calculated as the integral of the shaded triangle in the capacitor current shown in Fig. 3-6. So, the total charge can be written as:

$$\Delta q = \frac{1}{2}\left(\frac{T_S}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T_S \Delta i_L}{8} \qquad (3\text{-}10)$$

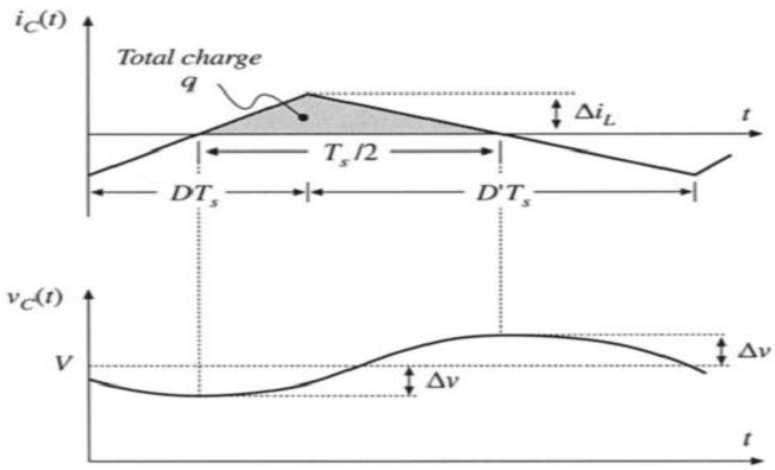


Fig. 3-6: Output capacitor current and voltage waveforms for buck converter [33].

Using Eq. (3-10), the output voltage ripple can be obtained as:

$$\Delta V_O = \frac{T_S \Delta i_L}{8\,C} \tag{3-11}$$

Substituting for Δi_L into (3-11) yields:

$$\Delta V_O = \frac{V_O}{8\,C\,L}(1-D){T_S}^2 = \frac{V_O(1-D)}{8\,C\,L\,{f_S}^2} \tag{3-12}$$

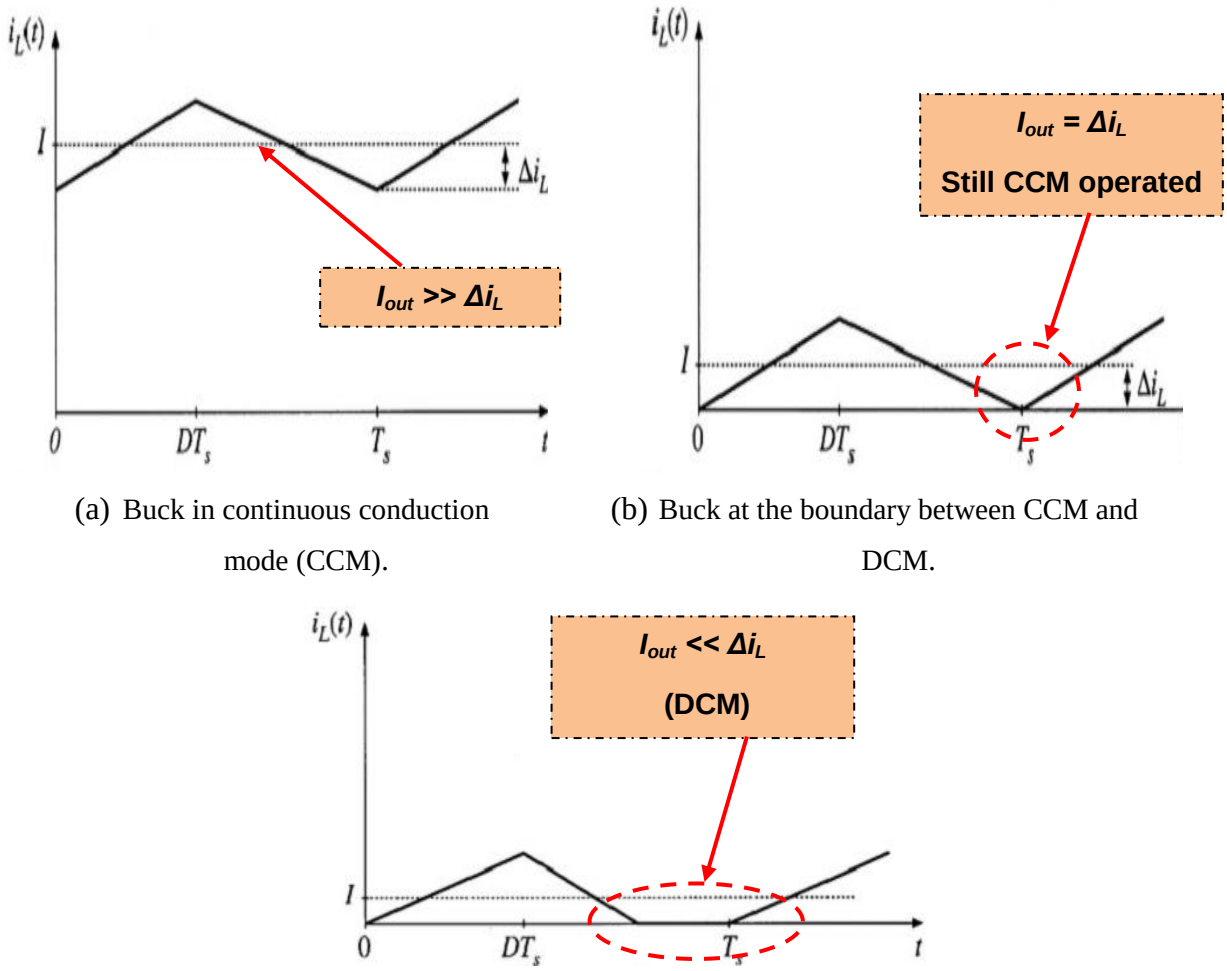
Eq. (3-12) is very useful in estimating the output voltage ripple for the ideal buck converter. The equation shows that output ripple can be decreased by using high capacitance value and high switching frequency. It is clear that the output ripple is independent on the load current.

3.3.2 Buck Converter Conduction Modes

With respect to the inductor current i_L, there are two types of conduction modes for buck converter: Continuous Conduction Mode (CCM), and Discontinuous Conduction Mode (DCM). The designation is determined based on the load current. If the load current is continuously maintained above zero for the entire period of operation, the converter is operating in CCM. If at any point in the cycle the load current falls to zero, the converter is operating in DCM. Separate sets of equations apply to each mode of operation to describe its behavior [34]. Fig. 3-7 illustrates the inductor current waveform at CCM, DCM and the boundary between them.

Eq. (3-6) predicts that the inductor current ripple is not depending on the output current. This means that the same current ripple is maintained whatever the value of the output load. Assume what happen when the load current decreases. As the inductor current ripple is not depending on the load, the DC component of inductor current decreases with the same ripple magnitude on it. If the load current continued to increase, the inductor current could reach a zero value in a way like the waveform shown in Fig. 3-7b.

Further decrease in the load current can lead to the extent that a new subinterval appears in each switching period like shown in Fig. 3-7c. This new subinterval happens when the inductor current reaches a zero value and become unable to reverse its direction and become negative.



(a) Buck in continuous conduction mode (CCM).

(b) Buck at the boundary between CCM and DCM.

(c) Buck in discontinuous conduction mode (DCM).

Figure 3-7: Inductor current of buck converter at different operation modes [33].

In order to ensure operation in CCM, a minimum inductance value should be used in the buck circuit. This minimum inductance assures that the inductor current will be always positive. The minimum inductance can be given by:

$$L_{min} = \frac{(1-D)V_O T_S}{2I_L} = \frac{(1-D)V_O}{2f_S I_L} \tag{3-13}$$

3.4 Pulse Width Modulation (PWM) Control For Buck Converter

The synchronous buck converter circuit shown in Fig. 3-1 is Vulnerable to changes due to input and load variations. To maintain a fixed output voltage, a closed loop control technique should be employed to control the system. The most common control method used in buck converter and voltage regulators is pulse width modulation (PWM). A simplified block diagram for the PWM controlled buck converter is shown in Fig. 3-8. The operation of the PWM control is based on monitoring the output voltage change and compensate for this change by adjusting the buck converter duty ratio. The duty ratio is adjusted in a way that guarantees a fixed output voltage at a predetermined value.

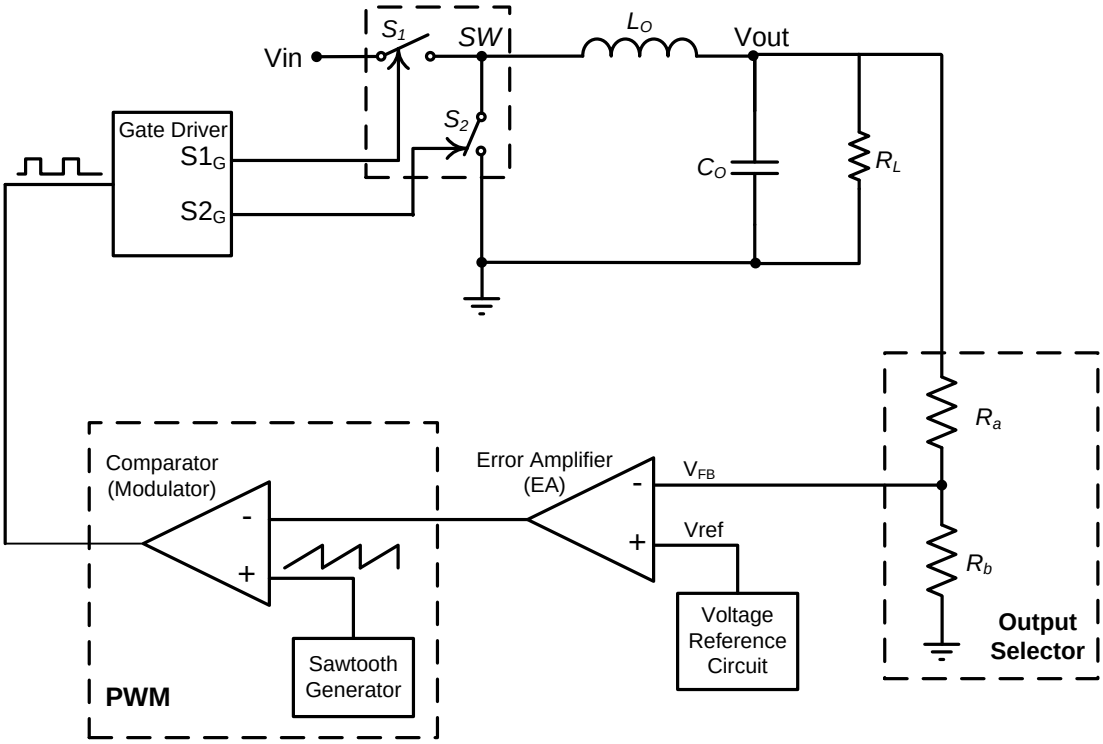


Figure 3-8: Buck converter with PWM control.

The sub-blocks of PWM control consist of a resistive voltage divider, error amplifier (*EA*), voltage reference circuit, voltage comparator, and saw-tooth generator. The operation of PWM control can be described briefly as following:

- A scaled version from the output voltage (V_{FB}) is taken by the resistive voltage divider formed by resistors R_a and R_b.

- The scaled output voltage (V_{FB}) is applied to the error amplifier. The error amplifier compares V_{FB} with a fixed voltage reference (V_{ref}) and amplifies the difference between them.

- The output of the error amplifier is compared with a saw-tooth signal. When the error signal is greater than the saw-tooth signal, the comparator output will be changed at logic "*high*" and vice versa.

- The output of the comparator is applied to the gate driver circuit where the logic "*high*" can be translated to turn-on S_1 and turn-off S_2 and vice versa.

- The saw-tooth signal has a fixed frequency and this frequency determines the switching frequency of the converter.

- As the saw-tooth has a fixed frequency, the comparator output will also have the same frequency but with a variable duty ratio.

- At steady state, the control loop will adjust the error signal to obtain a specific duty ratio from the comparator. This specific duty ratio is required to obtain a specific output voltage.

Fig. 3-9 shows how different error signals generate different duty ratios. It states that smaller error signal means that the output voltage is higher than the desired value. This means that the duty ratio should be lowered to encounter for this error. This is clear in case 1 as shown in Fig. 3-9. Unlike case 1, when the error signal value is higher, this means that the output voltage is lower than the desired value and the duty ratio produced will be high. This is illustrated by case 2 in Fig. 3-9.

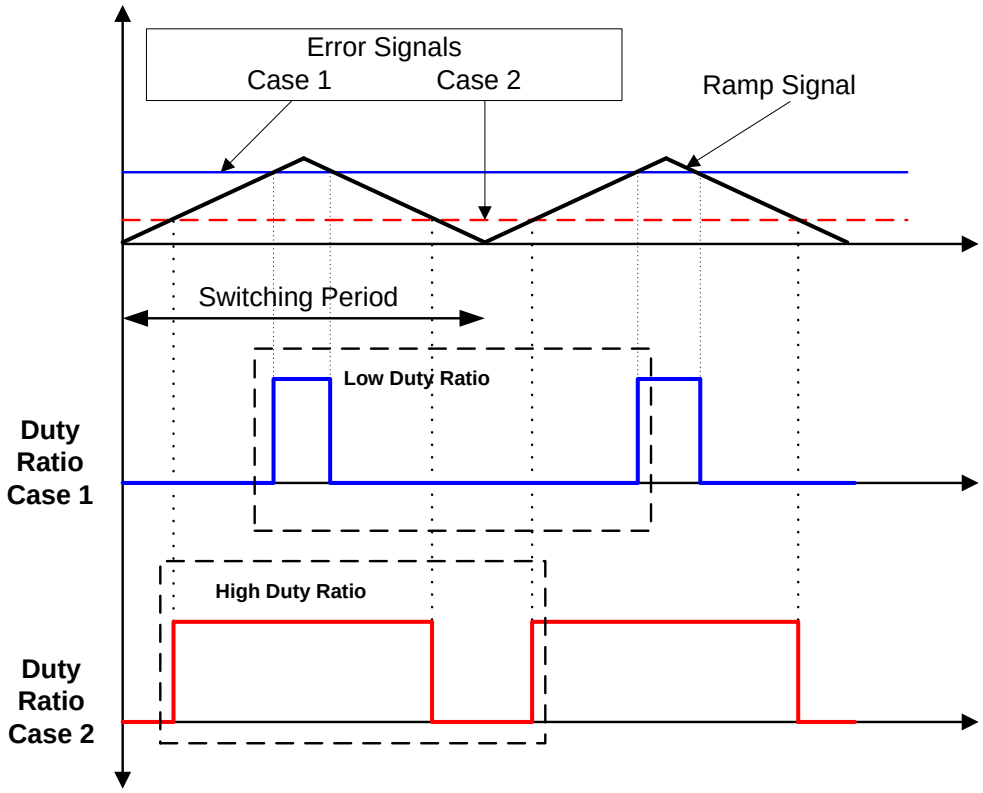


Figure 3-9: Pulse width modulation concept.

3.5 Power Losses in Buck Converter

The optimization for maximum efficiency at desired specifications can be reached by taking care of the converter power consumption. The power consumption of a buck converter is a combination of the conduction losses caused by the resistive parasitic impedances and the switching losses due to the capacitive parasitic impedances of the circuit components [35]. Listed below are the main sources of power dissipation.

3.5.1 Conduction Losses

The conduction loss sources are shown in the non-ideal model for buck converter in Fig. 3-10.

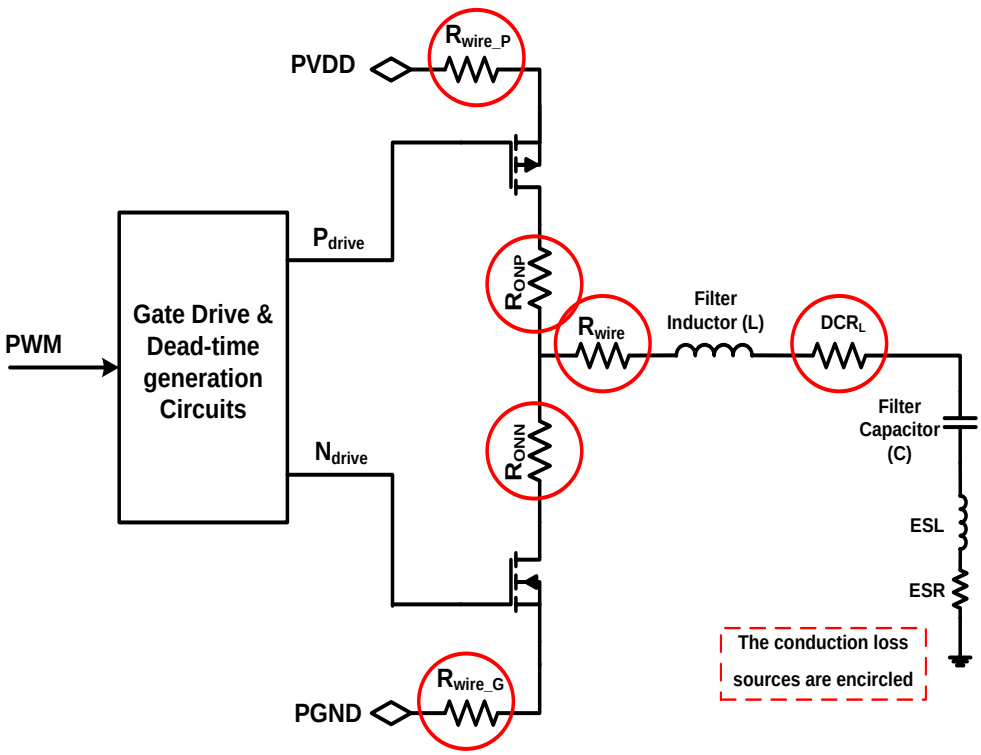


Fig. 3-10: Conduction loss sources in non-ideal buck converter.

The conduction loss can be calculated from the following equation:

$$P_{cond} = I_L^2.(R_{on} + DCR_L + R_{wire}) \quad (3\text{-}14)$$

where:

DCR_L: *the series resistance of the inductor.*

R_{wire}: *the total series resistance of trace pins and wirebonds on the output conduction pass.*

I_L: *the inductor rms current.*

The total on-resistance of the power switches R_{on} can be calculated by:

$$R_{on} = R_{on,P}.D + R_{on,N}.(1 - D) \quad (3\text{-}15)$$

where:

$R_{on,P}$: *the high side switch resistance.*

$R_{on,N}$: *the low side switch resistance.*

D: *the duty cycle.*

It is clear from Eq. (3-15) that the duty cycle determines which on-resistance will dominate; the PFET on-resistance or NFET on-resistance. The DCR_L effect can be minimized by choosing an inductor with a low series resistance.

3.5.2 Switching Losses

Switching loss is composed of several parts: MOSFET switching loss (high side and low side), MOSFET gate drive loss, low side body-diode loss, and MOSFET output capacitance loss.

I. MOSFET Switching Loss

The power MOSFET dissipates power during the turning-on and turning-off process. The turn-on switching loss can be calculated as following [28]:

$$P_{SW(FET,ON)} = \frac{1}{2} \cdot V_{in} \cdot I_{valley} \cdot \left(t_{sw(ON)}\right) \cdot F_{SW} \qquad (3\text{-}16)$$

where:

I_{valley}: *the inductor valley current*

$t_{sw(ON)}$: *the turn-on transition time*

The turn-off switching loss can be calculated as following [51]:

$$P_{SW(FET,OFF)} = \frac{1}{2} \cdot V_{in} \cdot I_{peak} \cdot \left(t_{sw(OFF)}\right) \cdot F_{SW} \qquad (3\text{-}17)$$

where:

I_{peak}: *the inductor peak current*

$t_{sw(OFF)}$: *the turn-off transition time*

The total MOSFET switching loss can be given by:

$$P_{SW(FET,total)} = P_{SW(FET,ON)} + P_{SW(FET,OFF)} \qquad (3\text{-}18)$$

It is clear from Eq. (3-16) and (3-17) that the MOSFET switching loss is depending mainly on the switching frequency. This means that as the switching frequency increases, the switching loss will increase too. The MOSFET switching loss is also depending on the parasitic capacitance of MOSFET. Using large size MOSFETs means high parasitic capacitance values, which in turn significantly increase the switching loss.

II. Gate Drive Losses

The gate drive loss can be given as following [28]:

$$P_{GD} = P_{gate\,(HS)} + P_{gate\,(LS)} = \left(Q_{g(HS)} + Q_{g(LS)}\right).V_{Driver}.F_{SW} \qquad (3\text{-}19)$$

where:

$Q_{g(HS)}$: *the total gate charge of the high-side MOSFET.*

$Q_{g(LS)}$: *the total gate charge of the low-side MOSFET.*

V_{Driver}: *the gate driver power supply voltage.*

F_{SW}: *the switching frequency.*

III. Body Diode Loss

In order to prevent the cross-conduction of the HS FET and LS FET (shoot-through), two short dead-times are added into the converter: rise edge dead-time between LS FET turn-off and HS FET turn-on and fall edge dead-time between HS FET turn-off and LS FET turn-on. During these two dead-time intervals, both the HS and the LS FETs are off, and LS FET body diode conducts the inductor current. The LS body diode conduction introduces two power losses into the system: dead-time loss (diode conduction loss) and diode reverse-recovery loss.

Dead-time loss is induced by low-side body diode conduction during dead-times and can be calculated using the following equation [28]:

$$P_{deadtime} = V_{BD} \times [(I_{out} - \frac{I_{ripple}}{2}) \times t_{deadtime(r)} + (I_{out} + \frac{I_{ripple}}{2} \times t_{deadtime(f)}].F_{SW} \quad (3\text{-}20)$$

where:

V_{BD}: the body diode forward voltage drop.

$T_{deadtime(r)}$: the dead time between LS MOSFET turn-off and HS MOSFET turn-on.

$T_{deadtime(f)}$: the dead time between HS MOSFET turn-off and LS MOSFET turn-on.

From Eq. (3-20), the body diode loss is depending on the output current, the dead-time periods and switching frequency. This type of power loss can be reduced by designing an optimum dead-time period. The dead-time

should not be too short in order to avoid turning on the two power MOSFETs at the same time. Also, the dead-times should not be too long, as the body diode of LS MOSFET will conduct for long time which increases the body diode loss for a significant value.

The second power loss that is introduced by the LS body diode is the reverse recovery loss. Reverse recovery loss happen during the time between the body diode being reversed and the turn-on of HS power MOSFET. Fig. 3-11 shows the reverse recovery loss of a diode.

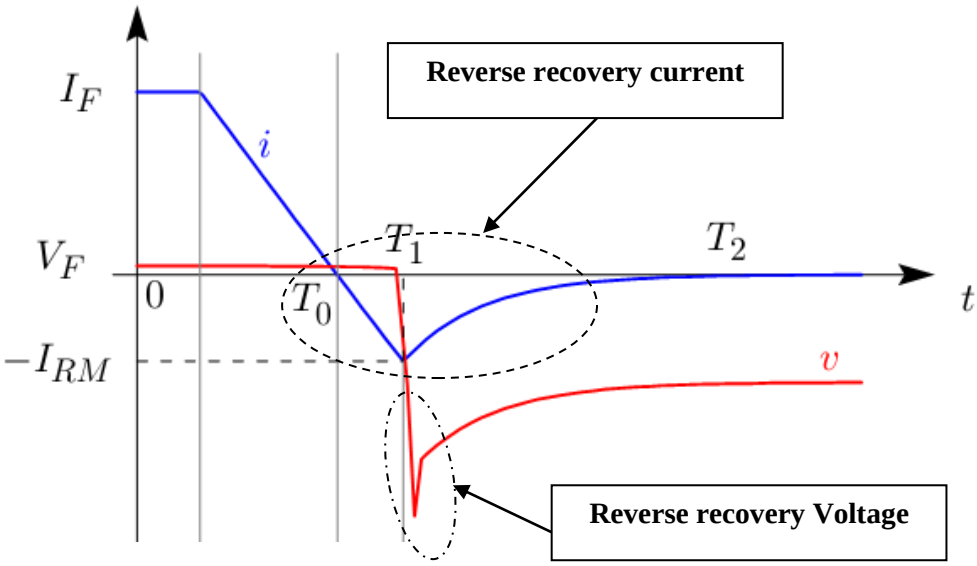


Fig. 3-11: PN diode turn-off results in reverse recovery waveforms [36].

The reverse recovery loss can be given as:

$$P_{Drr} = V_{IN}\, F_{SW}\, Q_{Drr} \tag{3-21}$$

where Q_{Drr} is the reverse recovery charge. Again, the reverse recovery loss can be minimized by decreasing the dead-time.

3.5.3 Inductor Related Power Loss

In addition to the conduction power loss due to the inductor DCR, there are other types of losses due to the inductor. These other types include the inductor core loss and the inductor AC resistance loss.

a. Inductor Core Loss

The energy loss in the inductor core can be identified as the difference between the energy applied to the core during the ON subinterval and the energy extracted from the core during the OFF subinterval in a switching system. The energy that is wasted in the core is called the "core energy loss". Normally, the inductor core loss is provided by the inductor supplier. If it is not available, it can be calculated using the following formula [37]:

$$P_{core} = K_1 \, f^x B^y \, V_e \quad (mW) \qquad (3\text{-}22)$$

where

V_e: *the effective volume of the core (cm^3).*

f : *the operating frequency (kHz).*

K_1, x, *and* y: *constants.*

The constants K_1, x, and y are unique to each core material.

b. Inductor AC Loss in Windings

The DC loss in inductor windings has been discussed before, where the *DCR* of the inductor is the source of power loss. As the switching frequency

increase a new phenomenon in the inductor windings appear. This phenomenon is called "*Skin Effect*".

The skin effect is caused by a changing *i(t)* within the conductor. The changing current induces a changing flux (*di/dt*) perpendicular to the cur-rent that induced it. According to Lenz's law, the changing flux induces eddy currents that induce a flux themselves, in opposition to the initial changing flux. The eddy currents are of a polarity opposite that of the initial current. The induced flux is strongest at the conductor's center and weakest at the surface, causing the current density at the center to decline from its dc value with increasing frequency. As a result, current gets pushed to the surface of the conductor, producing a lower current density at the center and a higher current density at the surface. Resistance increases because the resistivity of copper remains constant and the conductor's effective current carrying area decreases. The windings' ac resistance is found by determining the depth, known as penetration depth (or skin depth), to which current exists in the conductor at a particular frequency [38]. This depth can be calculated using the following equation:

$$D_{PEN} = \sqrt{\frac{\rho}{\pi . \mu . f}} \qquad (3\text{-}23)$$

where

ρ : *the resistivity of the inductor windings.*

μ : *the conductor's permeability.*

f : *the converter switching frequency.*

It is important to keep in mind that the inductor AC loss is due to an AC current only. In our application, the AC current is the inductor current ripple. The inductor DC current produces power loss in the inductor DCR only. The AC resistance of inductor can be given by:

$$R_{AC} = \rho \frac{L}{A} \tag{3-24}$$

where

ρ : *the resistivity of the winding material.*

L : *the conductor's windings length.*

A : *the effective conducting area.*

The effective conducting area can be considered as the surface area of conducting ring with thickness equal to the skin depth. Then Eq. (3-24) can be written as:

$$R_{AC} = \rho \frac{L}{[\pi\, r^2 - \pi(r - D_{PEN})^2]} \tag{3-25}$$

The inductor AC loss is due to the rms value of the AC inductor current (peak to peak ripple) flowing through the AC resistance.

3.6 Design Specifications For Buck Converter

In the next sections of this chapter, the main parts of a 2 MHz buck converter will be designed using a CMOS technology. The parts that will be designed have been shown in Fig. 3-8 which includes the power stage design, the gate driver circuit, the error amplifier, the PWM internal circuits, reference voltage generators, and the supply voltage generator.

The buck converter design should be capable of powering recent Intel Atom processor families. Such processors are requiring a voltage rail that varies between 0.75 V to 1.2 V. Recalling Fig. 1-7 that includes a summary for the power needs of Intel Atom ™ processors, the maximum power need is consumed by N500 series and approaches 8.5 W.

Based on our application, the buck converter design specification can be listed as following:

- Output voltage range 0.75 V to 1.5 V
- High output current capability up to 10 A
- High efficiency higher than 90%
- High switching frequency of 2 MHz
- Small output voltage ripple (<3%)
- Fast transient response (<5%)

The buck converter should be able to achieve these specifications. However, the design will be optimized at input voltage of 3 V, output voltage 1 V, output current of 6 A, and switching frequency of 2 MHz.

3.7 Power Stage Design

The power stage of buck converter is composed of these components that are responsible for processing, storing, and transferring the energy from the input to output. It is the core circuit of the converter. The power stage of buck converter has been described and its operation has been discussed. The buck converter's power stage is shown in Fig. 3-1. In this section, the design of the power stage components will be discussed in details and the predetermined specifications should be met.

3.7.1 Inductor Selection

For the advantages of CCM, the buck converter should be designed for CCM operation. In CCM, the inductor value is very critical. It is proven that there is a minimum inductor value should be used to ensure CCM operation. The minimum inductance is given in Eq. (3-4). Recalling the following:

$$L_{min} = \frac{(1-D)V_O}{2f_S I_L}$$

where:

L_{min} :	*is the minimum inductance value for CCM.*
D:	*is the duty cycle (1 V/3 V).*
f_{sw}:	*is the switching frequency (2 MHz).*
V_{out} :	*is the desired output voltage (1 V).*
I_{load}:	*is the required output current (1 A).*

The required output current (1 A) is not the maximum output current for the buck converter. This value is the lowest value that the converter can operate

in CCM. So, the minimum inductor value from the equation is 167 nH. For safety, the inductor value is chosen to be higher than 167 nH. An inductor with a value of 220 nH from Vishay is selected and the dimensions of this inductor are shown in Fig. 3-12. All the dimensions shown are in inches/mm. The selected inductor has a maximum DC resistance of 5.2 mΩ.

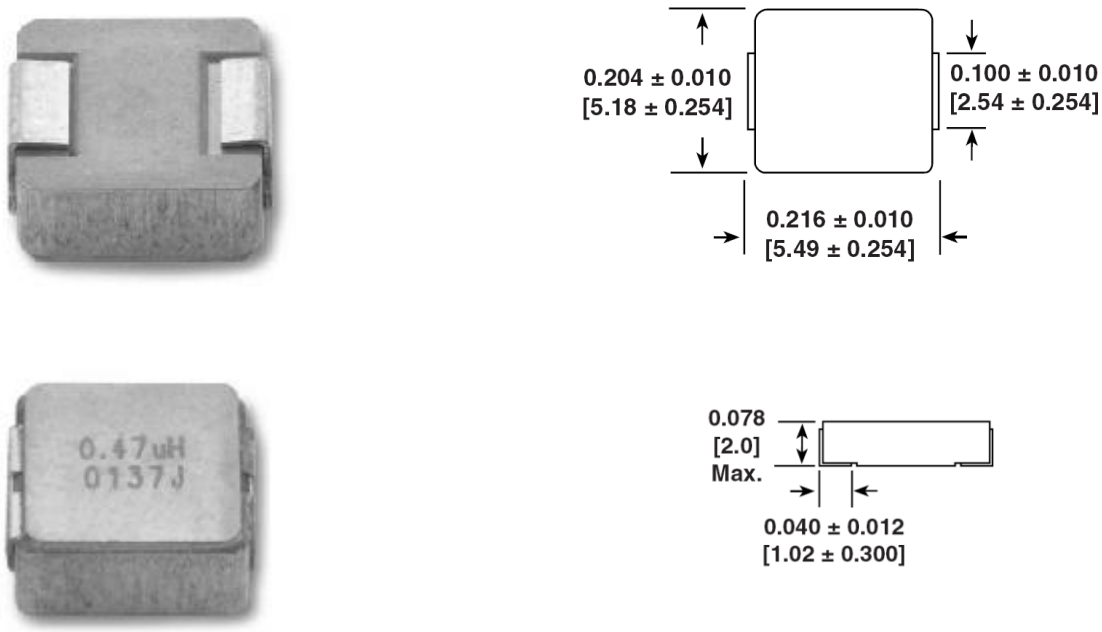


Figure 3-12: The selected one-turn IHLP-2020BZ-01 inductor [39].

3.7.2 Output Capacitor Selection

The output capacitor value is an important part in the filtering operation of output voltage. The output capacitor is not only required for decreasing the output ripple, but it also affects the buck converter undershoots/overshoots too. The undershoot/overshoot can be defined as the deviations that happen in the output voltage from the nominal DC value due to sudden step change

in output load. The concept of undershoot/overshoot can be illustrated by Fig. 3-13.

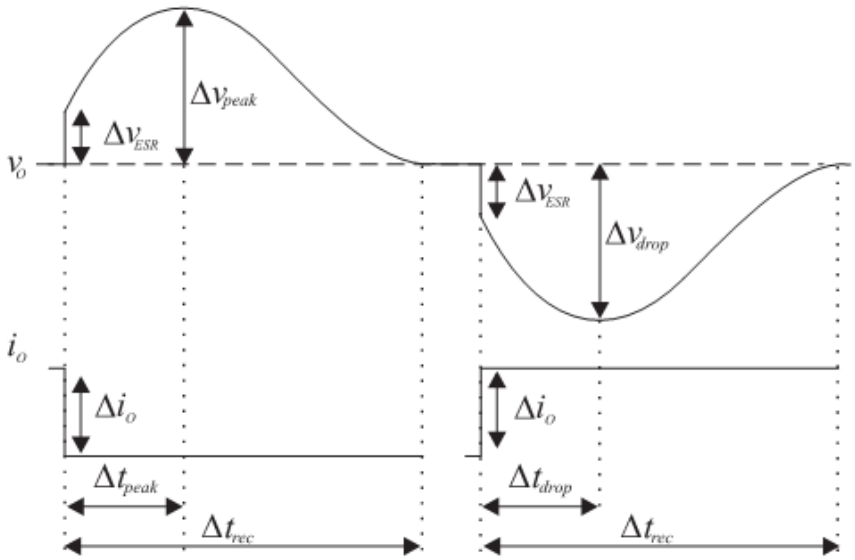


Figure 3-13: Conceptual transient response in buck converter [40].

As described in the figure, a step-up change in the output current i_o results in an undershoot in the buck's output voltage. Opposite to that, the step-down change results in an overshoot in buck's output voltage. This phenomenon can be explained by the help of Fig. 3-4 as following:

Recall that,

$$i_L = i_C + i_O \qquad (3\text{-}26)$$

Suppose what happen when a step-down sudden change in the output current occur. As the inductor current cannot change instantaneously, the step-down change in the output current will make the inductor current I_L higher than the load current I_O momentarily. According to Eq. 3-26, the

current difference between the old value of I_L and the new value of I_O will flow through the capacitor which creates an overshoot on the output capacitor voltage. The output voltage undershoot can be explained by the same way by the help of Eq. (3-26). Since overshoot/undershoot percentage is inversely proportional to the output capacitor value, a high capacitance value could help in minimizing undershoot/overshoot percentage.

Based on the maximum output ripple specification of 3%, the minimum output capacitor value is calculated from Eq. (3-12) and the obtained value is 6 µF. Unfortunately, this capacitance value is sufficient if the capacitor is ideal and of course there is no ideal capacitor. The capacitor's ESR and ESL values have a big effect on the output ripple which should be taken into consideration. To describe the effect of capacitor's ESR and ESL, consider the circuit shown in Fig. 3-14.

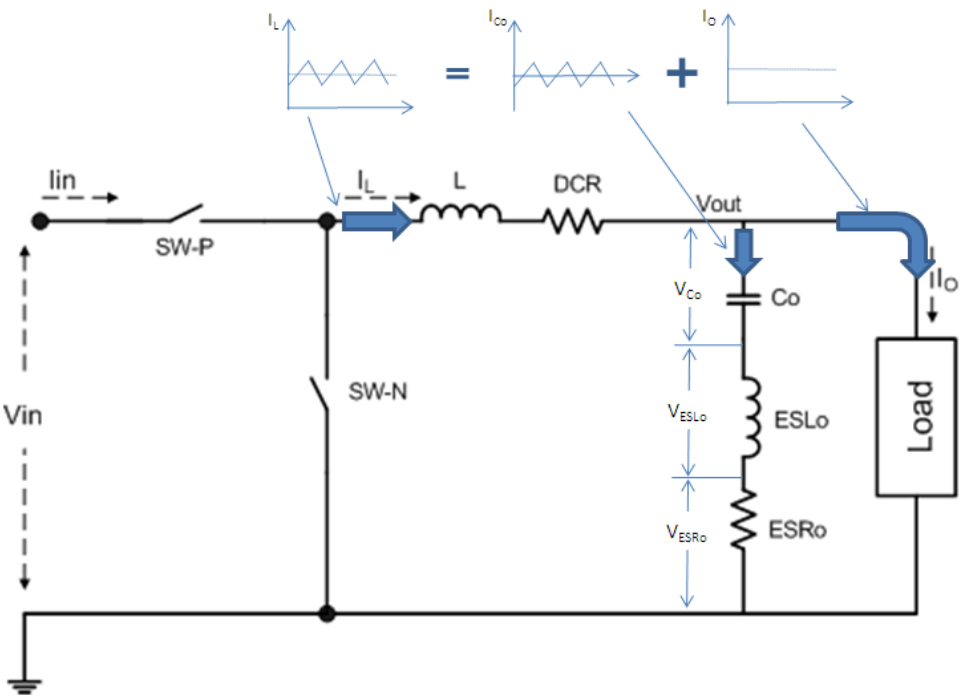


Figure 3-14: The effect of capacitor's parasitic on output ripple [25].

As illustrated in the figure, the inductor current ripple is passing through the output capacitor. Of course, the inductor current has a triangular shape. This triangular shaped current passes through three components which are the capacitor itself, its ESR, and its ESL. So, three voltage components will be produced can be given by the following equations [25]:

$$V_{Co} = \frac{1}{C_O} \cdot \int_0^T i_{Co}(t)dt \tag{3-27}$$

$$V_{ESLo} = ESL_o \cdot \frac{d}{dt} i_{Co}(t) \tag{3-28}$$

$$V_{ESRo} = i_{Co}(t).ESR_O \tag{3-29}$$

If the capacitor current has a triangular shape, the shape of the voltage for each component can be concluded as following:

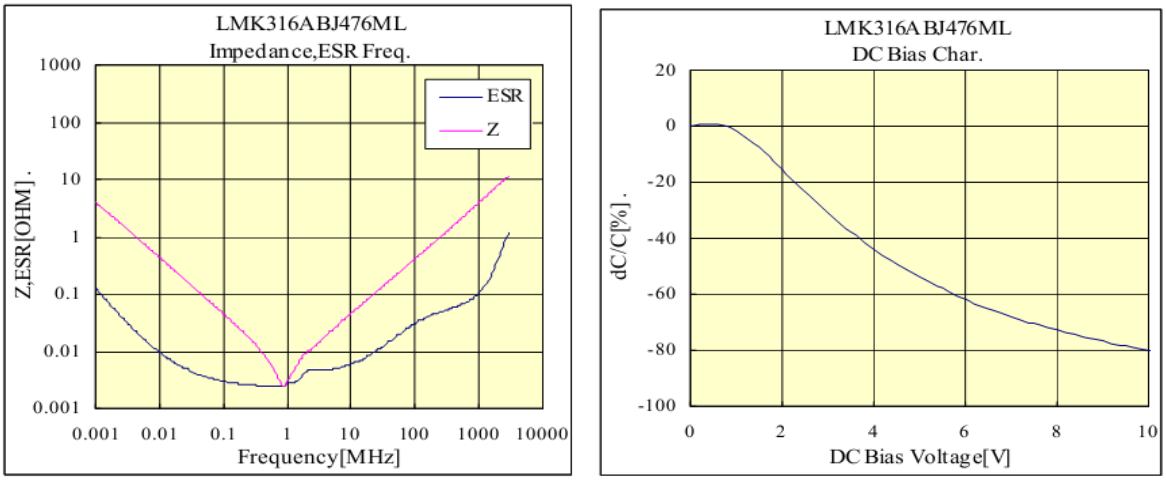
- The voltage across the capacitor has a second order shape.
- The voltage across the capacitor's ESR has a triangular shape.
- The voltage across the capacitor's ESL has a square-wave shape.

The actual output voltage ripple will be the sum of these voltage components:

$$\Delta V_O = V_{Co} + V_{ESLo} + V_{ESRo} \tag{3-30}$$

It states that higher ESR and ESL values will result in higher output ripple percentage. In order to decrease the effect of capacitor's parasitic, two paralleled 47 µF capacitors are used in order to minimize the output ripple

and the output undershoot/overshoot at the same time. Fig. 3-15 shows the output capacitors impedance, ESR, and capacitance variation due to the applied DC voltages.



(a) Impedance and ESR vs. Frequency of LMK316BJ476ML-T capacitor.

(b) DC biasing characteristics of LMK316BJ476ML-T capacitor.

Figure 3-15: Impedance, ESR, and capacitance variation due to DC voltages for selected capacitor [41].

3.7.3 Power MOSFETs Design

How to design the power MOSFETs has been defined previously in chapter two. Once again, the power MOSFETs' width should be selected in a way that guarantees the maximum allowable efficiency at the specified conditions.

We know that the conduction loss is inversely proportional to the power MOSFETs' width. One can make the power MOSFETs very wide in order to get the minimum conduction loss. In this way, two other important factors will be affected which are the power MOSFETs' size and the switching loss. If the MOSFETs are made wider, this means that the die size will be increased. In addition, wide MOSFETs have higher parasitic capacitances which increase the switching losses in the other side. The trade-off between the power MOSFETs' size and power loss should always kept in mind. As the main target of our converter is the high efficiency, increasing the die size by few millimeters is not the issue.

The designed buck converter has a wide range of load current that extends from 1 A to 10 A. POL converters are concerned by operating efficiently at heavy load currents. The converter should be designed to have a maximum efficiency at midpoint in the load current range which is 6 A. In addition, the efficiency values at all the points of the range should be acceptable and are not far from the maximum point. At these heavy loads, the conduction losses will be the dominant source of power loss. So, the power MOSFETs' size can be increased without worry about the switching losses as their values will be smaller than the conduction losses.

A scan over a wide range of MOSFET's widths has been done and from the curve the optimum MOSFET's width can been selected. It is important to note the duty ratio is smaller than 50% and from Eq. (3-15) that the power NMOS on-resistance will be more effective than power PMOS on-resistance. The selection of the power NMOS and PMOS is started from a 440 mm for NMOS and 320 mm for PMOS, and then the width of power MOSFETs is changed around the start point until the maximum efficiency is obtained. Fig. 3-16 shows the efficiency versus the width of power MOSFETs.

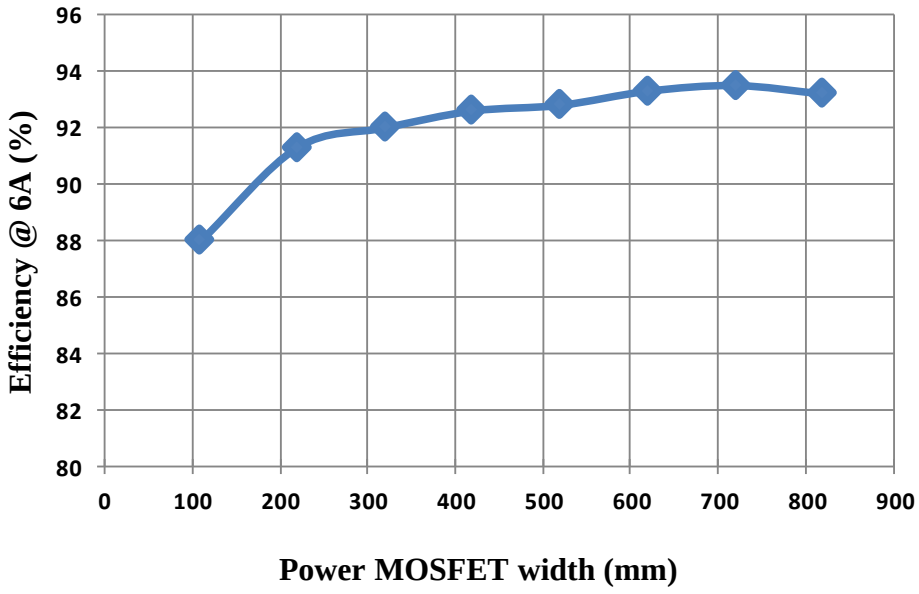


Figure 3-16: Efficiency vs. power MOSFETs width at 6 A load current.

A maximum efficiency of 93.5% is reached at PMOS width of 720 mm as shown in Fig. 3-16. This is the optimum MOSFETs width that can be used.

3.8 Error Amplifier Design

The error amplifier (*EA*) is simply an operational amplifier (*Op Amp*). The EA is an important part in the PWM closed-loop system. The *EA* has two inputs that accept two signals; a scaled version from output voltage (V_{FB}) and a constant reference voltage (V_{ref}). The resistive divider (R_a, R_b) is responsible for obtaining V_{FB} from the output voltage. The design of R_a and R_b is done in a way that makes V_{FB} is equal to V_{ref} if the output voltage is at the desired value. The *EA* is concerned by detecting the difference between V_{ref} and V_{FB}. This difference is called "*error signal*". This error signal is applied to the *PWM* and the *PWM* is responsible for generating a duty ratio relevant to the error signal.

In order for the buck converter to operate properly at high switching frequencies, produce accurate output voltage, and has fast transient response, an important requirements in the *EA* design should be considered such as:

- High gain.
- Wide bandwidth.
- High slew rate.

Many EAs that can be used as a part of the closed-loop buck converters have been presented in literatures. For our application, ultra-high performed EAs would be complex and power consuming. One of the most common *EA* topologies is the two-stage Op Amp. The two-stage Op Amp can give a relatively high gain, high bandwidth, low power consumption and enough slew-rate. Also, it can be easily stabilized as it is composed simply from two stages. So, the two-stage Op Amp is suitable for our application.

The two-stage Op Amp circuit is shown in Fig. 3- 17. As shown, the first stage is a differential amplifier like any other Op Amp and the second stage is a common source amplifier. Basically, the two-stage Op Amp has three topologies: PMOS differential pair, NMOS differential pair, and PMOS/NMOS composite differential pair. Generally, PMOS differential pair is preferred because it optimizes slew rate, unity-gain frequency, and minimizes noise.

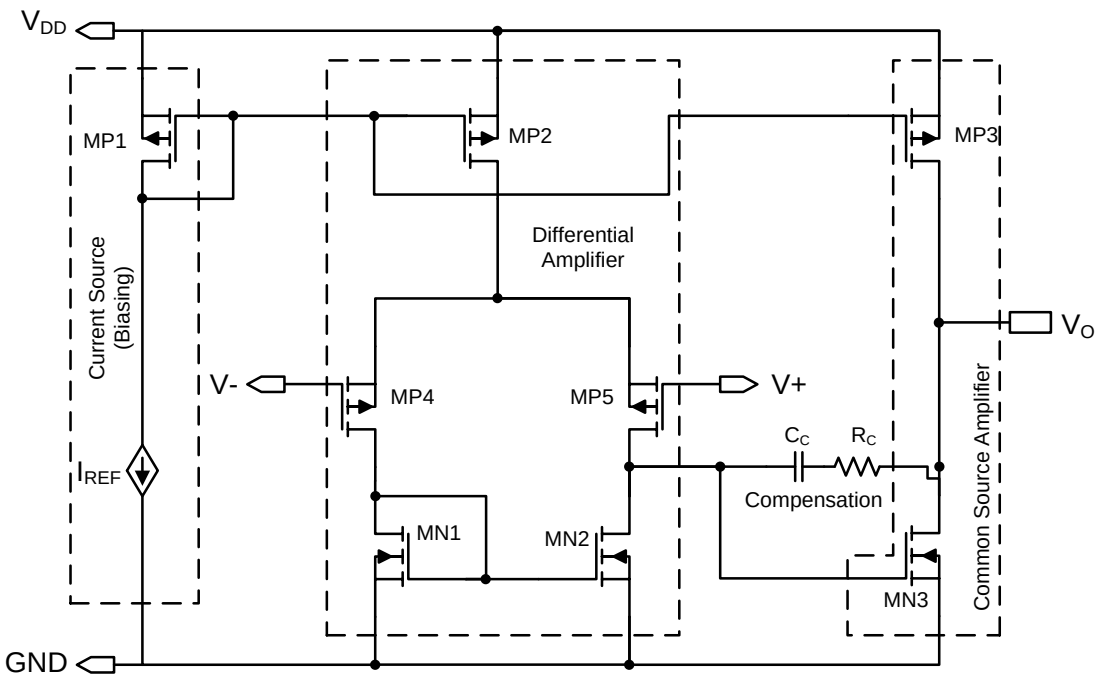


Fig. 3-17: PMOS differential pair Op Amp circuit.

The total gain of the Op Amp is the multiplication of individual gain of each stage. The gain of the differential amplifier stage can be given as:

$$A_{vd} = g_{mp5}(r_{dsp5} \parallel r_{dsn2}) \tag{3-31}$$

where:

A_{vd}: *is the differential amplifier gain.*

g_{mp5}: *is the trans-conductance of transistor MP5.*

r_{dsp5}: *is the drain-source resistance of MP5.*

r_{dsn2}: *is the drain-source resistance of MN2.*

where the trans-conductance of any PMOS transistor can be given as:

$$g_m = \mu_p C_{ox} \frac{W}{L}(V_{SG} - |V_{tp}|) \tag{3-32}$$

where:

μ_p: *is the mobility of holes.*

C_{ox}: *is the gate capacitance per unit area.*

V_{GS}: *is the gate-source voltage.*

V_{tp}: *is the threshold voltage.*

There are some constant parameters that depend on the technology such as μ_p ,C_{ox} and V_{tp}. There is no control on these parameters and they should be supplied in the technology datasheets. This implies that the trans-conductance can be adjusted by designing *W/L* and V_{GS}.

The drain-source resistance of any PMOS transistor can be expressed as:

$$r_{dsp} = \frac{2L}{\lambda\, \mu_p C_{ox} W (V_{SG} - |V_{tp}|)^2} \qquad (3\text{-}33)$$

where:

λ: *is the channel length modulation parameter.*

W: *is the transistor width.*

L: *is the transistor channel length.*

Eq. (3-33) implies that the drain-source resistance is inversely proportional to *W/L* which is opposite to the trans-conductance of the same transistor. So, if *W/L* ratio is increased, it will increase the trans-conductance and decrease the drain-source resistance at the same time. The *W/L* ratio should be designed to give suitable values for trans-conductance and drain-source resistance that give a satisfied gain.

The gain of the common source amplifier:

$$A_{vCS} = g_{mn3}(r_{dsn3} \parallel r_{dsp3}) \qquad (3\text{-}34)$$

where:

A_{vCS}: *is the gain of common source amplifier.*

g_{mn3}: *is the trans-conductance of transistor MN3.*

r_{dsn3}: *is the drain-source resistance of MN3.*

r_{dsp3}: *is the drain-source resistance of MP3.*

where the trans-conductance and source-drain resistance of any transistor can be given by Eq. (3-32) and (3-33), respectively.

The total gain of the two-stage Op Amp is the multiplication of Eq. (3-31) and (3-34) and it is given by:

$$A_v = g_{mp5} g_{mn3} (r_{dsp5} \parallel r_{dsn2})(r_{dsn3} \parallel r_{dsp3}) \qquad (3\text{-}35)$$

The compensation network shown in Fig. 3-17 is used to ensure the Op Amp stability if the Op Amp is configured as a closed-loop. The compensation type used in our Op Amp circuit is called "*Miller compensation*". The compensation network is composed of a capacitor C_C and a resistor R_C. The small signal model of the two-stage Op Amp with miller compensation is shown in Fig. 3-18.

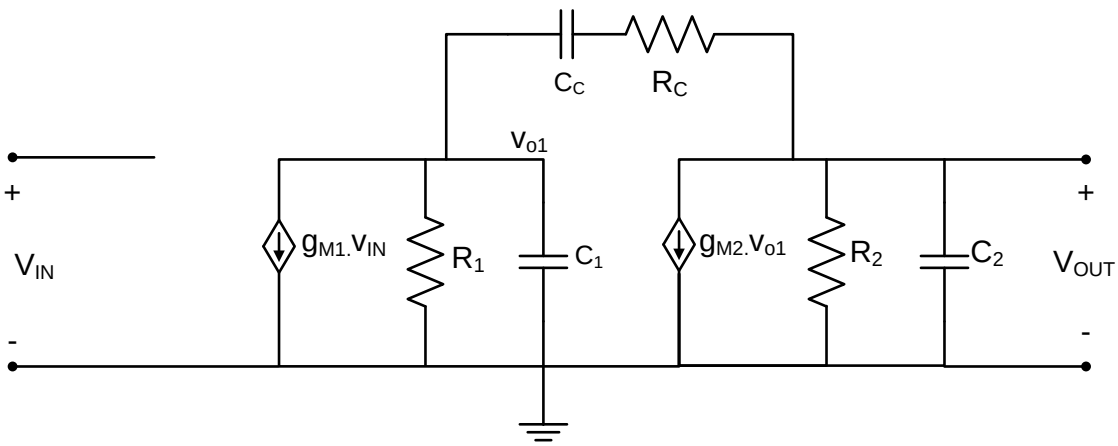


Figure 3-18: Small-signal model for two-stage Op Amp [56].

From Fig. 3-18, it is clear that the Op Amp circuit have two poles. One pole is at the output of the first stage and the second pole at the output of the second stage. Without compensation the two poles' location can be given by:

$$P_1 = \frac{-1}{R_1 C_1} \qquad (3\text{-}36)$$

where:

C_1: *is the equivalent output capacitance of first stage.*

R_1: *is the equivalent output resistance of first stage.*

And the second pole location can be given as:

$$P_2 = \frac{-1}{R_2 C_2} \tag{3-37}$$

where:

C_2: *is the equivalent output capacitance of second stage.*

R_2: *is the equivalent output resistance of second stage.*

The main idea behind miller compensation is to relocate the poles' position in order to obtain a satisfied phase response and stable system. The effect of adding the miller capacitance can be explained by giving the poles' position after adding C_C [42].

$$P_1 \cong \frac{-1}{g_{m2} R_1 R_2 C_C} \tag{3-38}$$

And the position of the second pole can be given as:

$$P_2 \cong \frac{-g_{m2} C_C}{C_1 C_2 + C_2 C_C + C_1 C_C} \cong \frac{-g_{m2}}{C_1 + C_2} \tag{3-39}$$

The effect of miller compensation can be now clearly described. Comparing Eqs. (3-36) and (3-38) show that the position of the first pole is moved toward lower frequencies; i.e. the pole is moved toward the origin of the *S* plane. By the same way, Eqs. (3-37) and (3-39) show that the second pole is moved toward high frequency; i.e. the pole is moved away from the

origin of the *S*-plane. Fig. 3-19 shows the gain and phase response for uncompensated and miller compensated Op Amp.

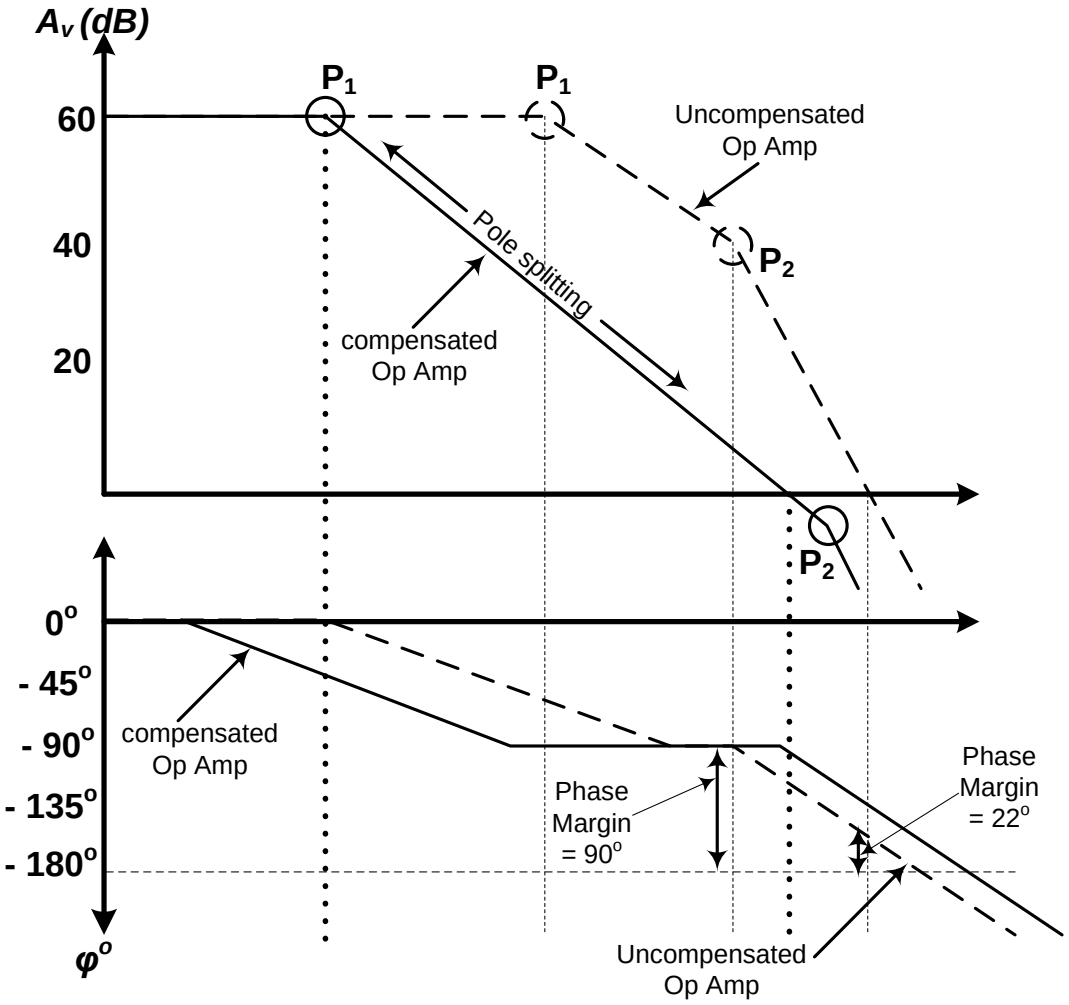


Figure 3-19: Gain and phase response of compensated and uncompensated OpAmp

The enhancement in the phase response is clear in Fig. 3-30 in the sacrifice of the Op Amp bandwidth which becomes lower after compensation. According to Eq. (3-38) and (3-39), as the miller capacitance value is increased the two poles are split from each other and further improvement in the phase response can be achieved. This is explained by the H-spice based simulation results shown in Fig. 3-20.

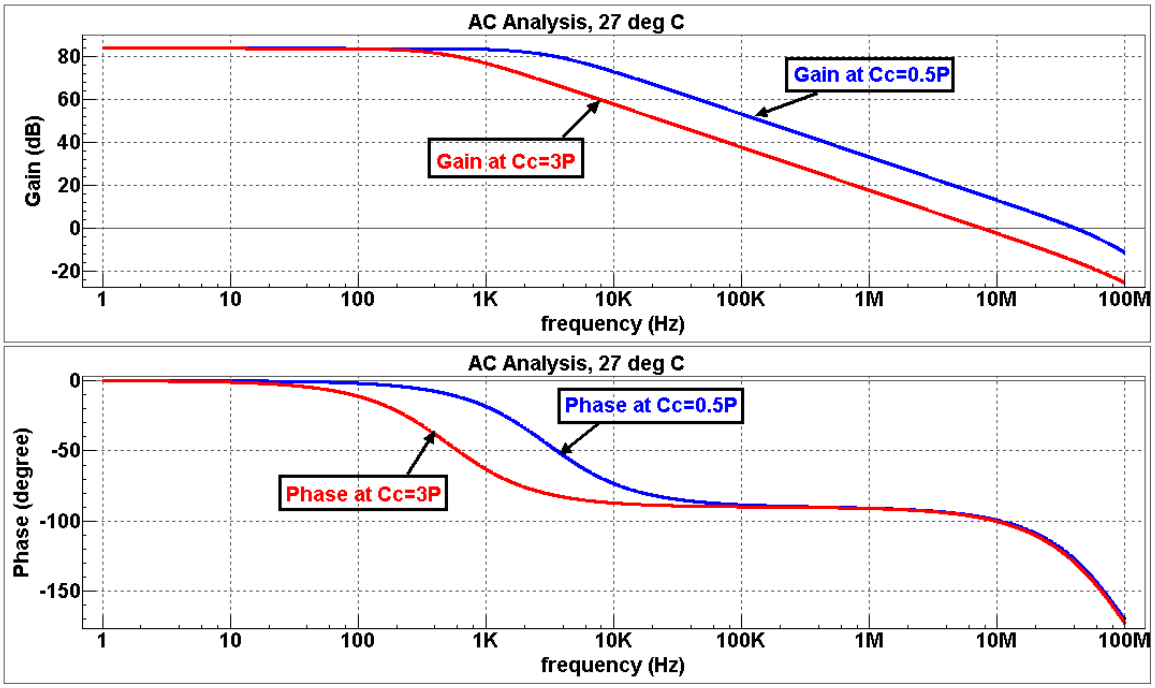


Figure 3-20: Miller capacitance effect on OpAmp's gain and phase.

The miller capacitor creates a zero in the right half of *S*-plane (*RHP*). Of course this *RHP* zero is undesirable because it has the effect of a left half plane (*LHP*) zero on that gain and the effect of *LHP* pole on the phase. In other words, the *RHP* zero will boost the gain which delays the gain crossing with 0 dB and will decrease the phase. The result will be poor phase margin. This *RHP* zero can be eliminated by designing the resistor R_C and zero location can be given by:

$$Z = \frac{1}{C_C.\left(\frac{1}{g_{m2}} - R_C\right)} \tag{3-40}$$

It is obvious from Eq. (3-40) that the zero is located in the *RHP*. Good improvement in the phase response can be obtained if R_C is made greater than $1/g_{m2}$. This will move the zero to the *LHP*.

The two-stage Op Amp circuit is designed and simulated. The simulation results show that a minimum DC gain of 82.8 dB can be obtained. The maximum unity gain bandwidth (UGB) is more than 10 MHz and more than 60 degree of phase margin is achieved. Fig. 3-21 shows the simulation results with varying supply voltage, temperature value, and process node.

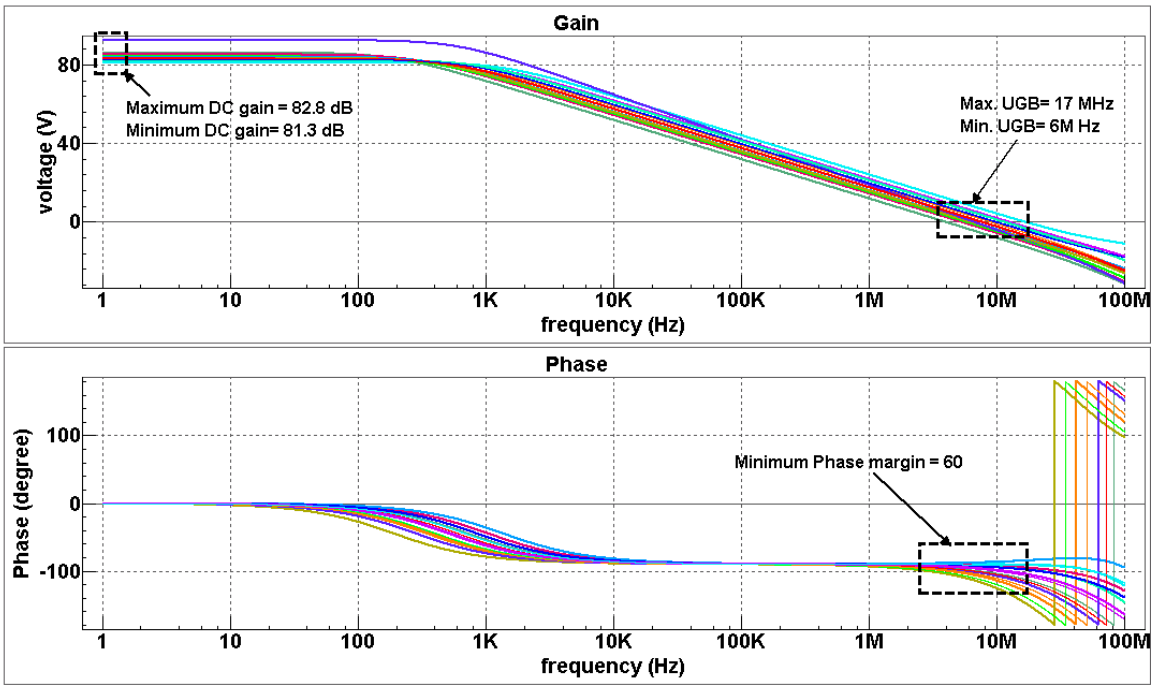


Figure 3-21: Two-stage Op Amp gain and phase with supply [±10%] and Temperature [-40, 25 and 125 C] and process node variations.

3.9 Triangular Signal Generator

The triangular signal is a main part of the PWM circuit. The triangular signal is compared with the error signal and the duty cycle is produced upon on the comparison. The triangular signal generator is the circuit that produces the triangular signal with a specific amplitude and specific frequency. The main idea of generating triangular signals is to charge and discharge a capacitor with a constant current. The voltage across the capacitor will be a triangular-shaped signal. The block diagram of the triangular signal circuit is shown in Fig. 3-22. The two comparators are used to limit the peak-to-peak value of the triangular signal. The output of the comparators are applied to a logic RS latch that command the current source circuit to charge or discharge the capacitor.

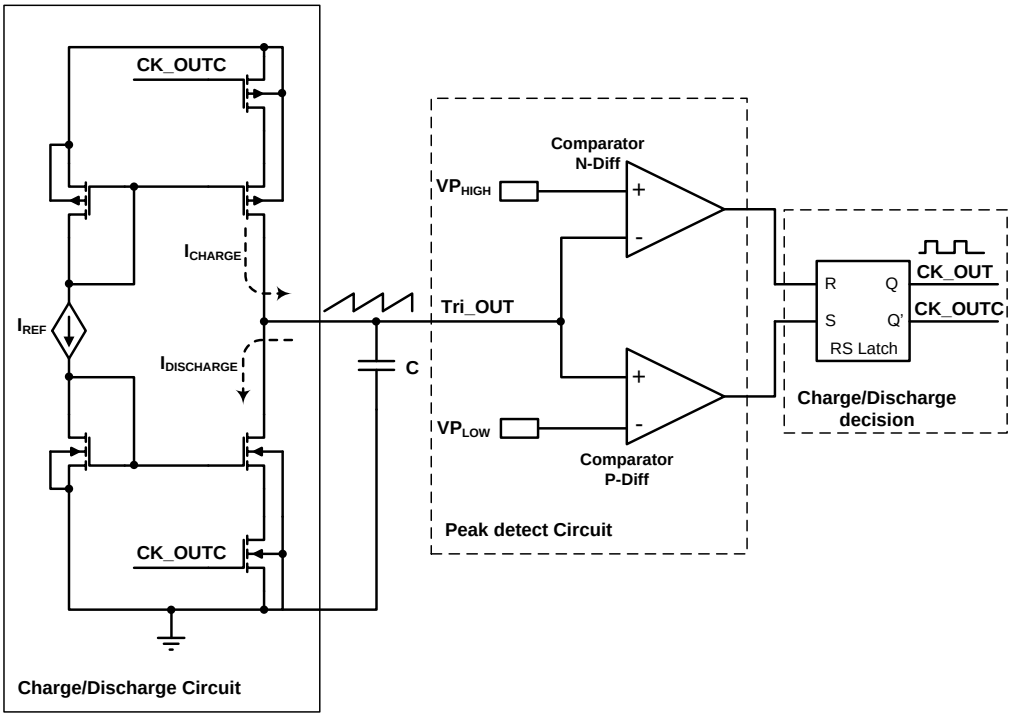
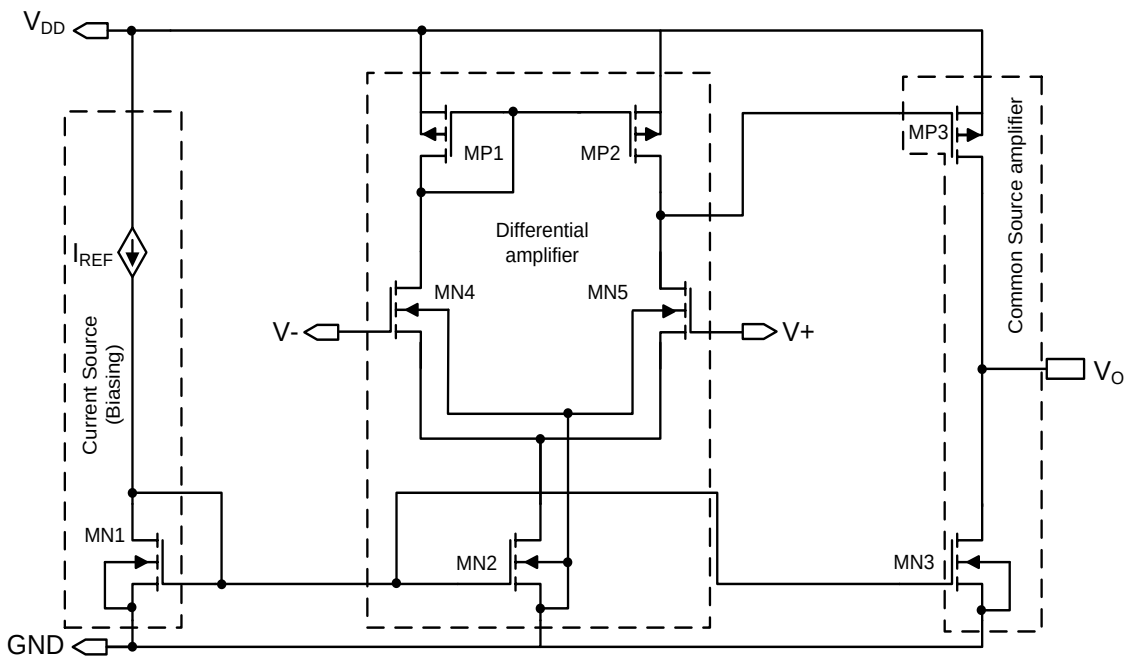


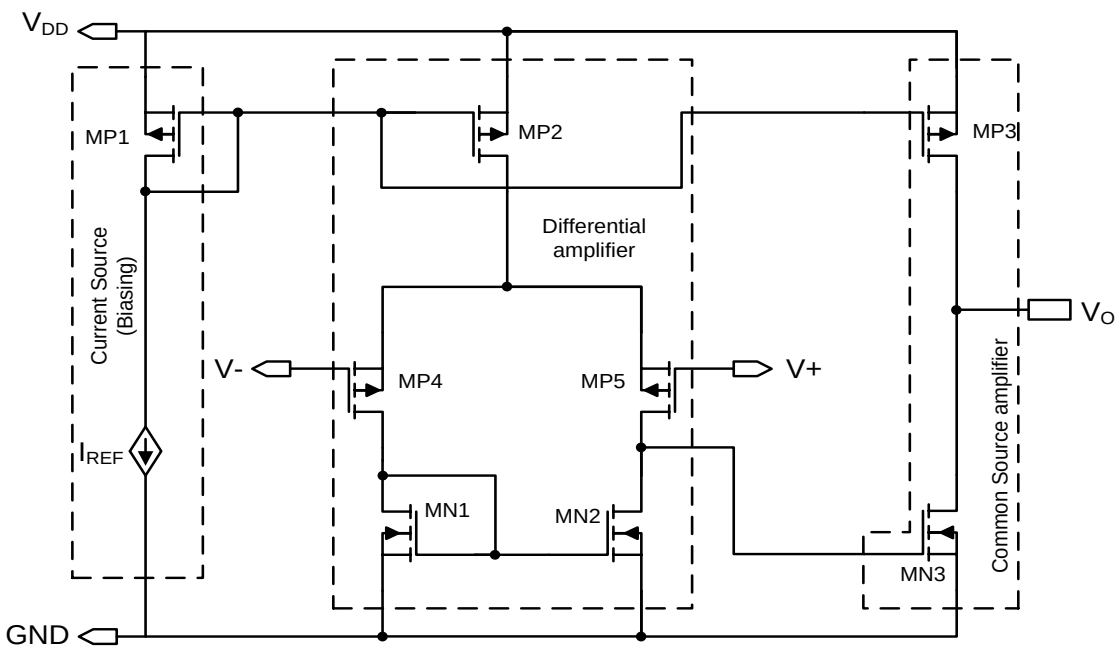
Figure 3-22: Block diagram of triangular signal generator circuit.

There are two topologies of comparators that are used in "*Peak Detect Circuit*". The first one is named "*Comparator N-diff*" and the second one is named "*Comparator P-diff*". The topology "*Comparator N-diff*" is using NMOS transistors for the differential input pair and "*Comparator P-diff*" is using PMOS transistors for the differential input pair. Using NMOS transistors is more accurate and fast for high values of input voltage, so "*Comparator N-diff*" is used to detect the high peak of the triangular signal. On the other hand, PMOS transistor would be helpful for low values of input voltage, so "*Comparator P-diff*" is used to detect the low peak of the triangular signal.

The two stages topology is used to implement the two comparators as it is the simplest topology for our application. The schematic diagrams of the designed comparators are shown in Fig. 3-23.



a) Two-stage N-diff comparator circuit



b) Two-stage P-diff comparator circuit

Figure 3-23: Schematic circuits of designed comparators.

The comparators shown in Fig. 3-23 are designed and implemented in CMOS technology. The simulation result of AC response for the two comparators is shown in Fig. 3-24. The simulation results show that the gain of "*Comparator N-diff*" and "*Comparator P-diff*" is 76 dB and 83.1 dB, respectively. The result shown is simulated at the room temperature and nominal process condition.

After designing the comparators, the complete circuit of triangular signal generator is designed for a 2 MHz output frequency. The simulation result for the triangular signal and the clock signal is shown in Fig. 3-25. The value of the output frequency can be adjusted after fabrication by proper trimming for the current reference circuit with predetermined values.

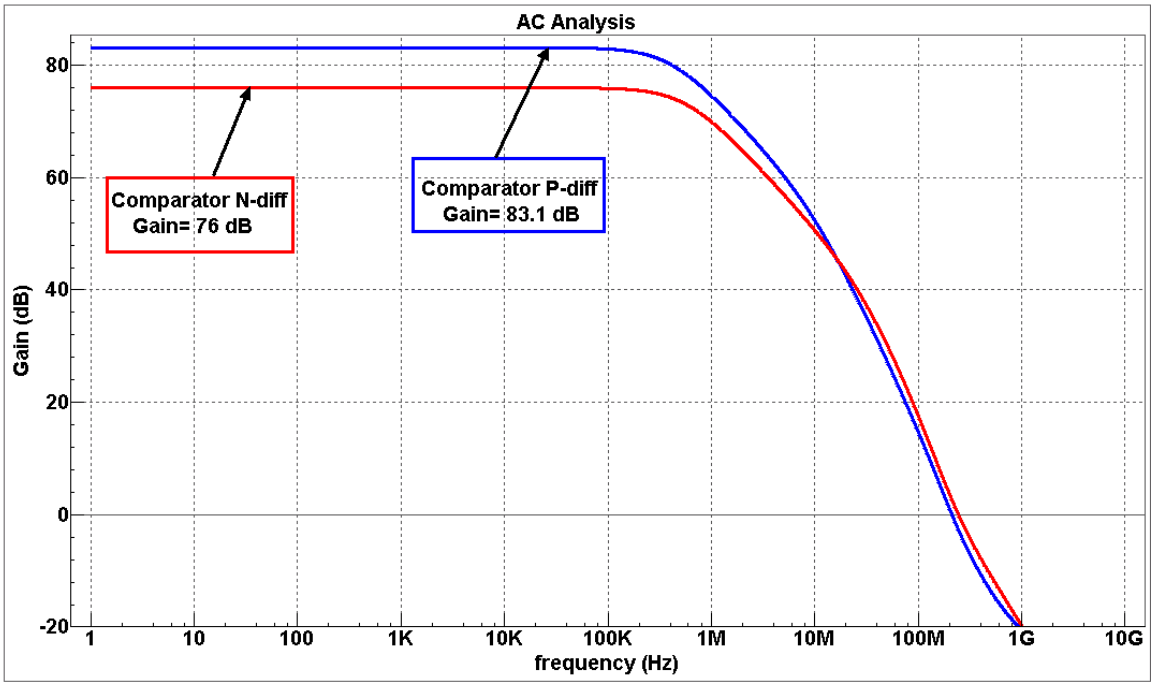


Fig. 3-24: Gain vs. frequency for the designed two-stage comparator.

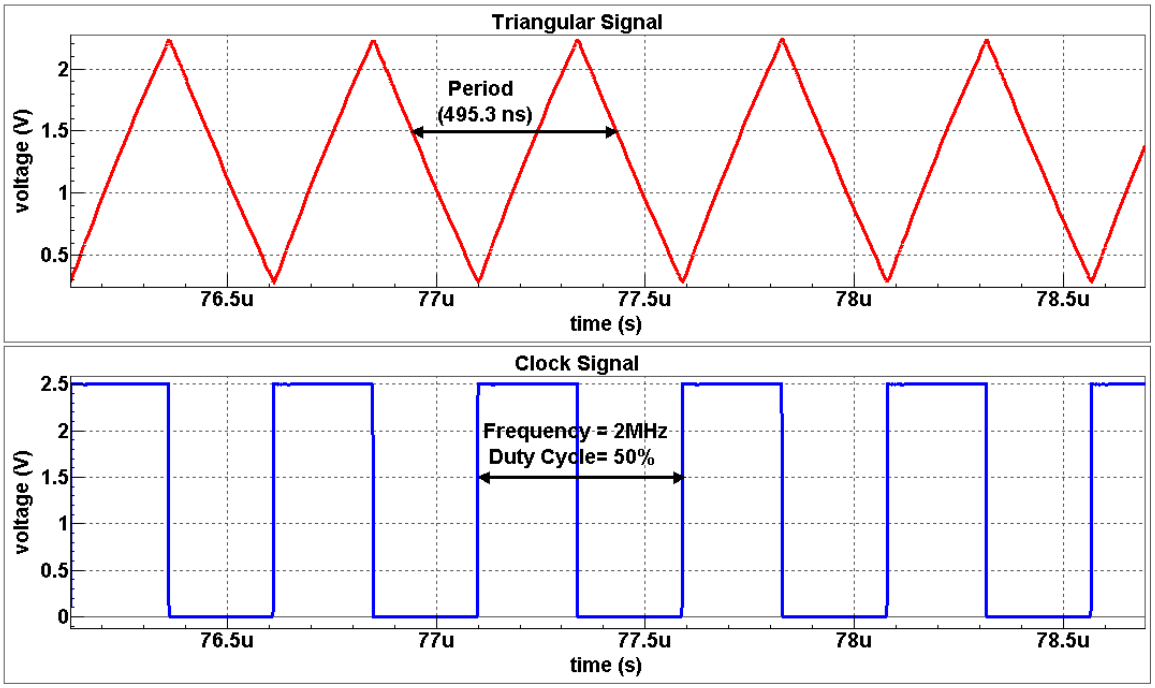


Figure 3-25: Simulation result for triangular signal and clock signal.

3.10 Design of PWM's Comparator

The voltage comparator is used in the PWM controller to generate the required duty cycle for the buck converter. The voltage comparator compares the triangular signal with the error signal. It is mentioned previously how the result of comparison should be.

Many topologies can be used to realize such comparator. One of such topologies is the two-stage Op Amp after removing the compensation network. The compensation network is removed as there is no feedback will be employed and phase margin become with no meaning. The two-stage Op Amp is the simplest topology for realizing comparator but still has some limitations. To obtain a wide range of duty cycles, the comparator should be able to respond accurately, has small offset voltage, and respond fast over a wide range of input voltage. Suppose what happen if the pre-described "*N-diff Comparator*" topology is used. The comparator would be able to respond in a fast way and accurately at high input values. At low input values, the differential pair devices will be pulled out of their active region and the gain dramatically drops to lower values. By the same manner, "P-diff Comparator" topology shows a satisfactory response at low input values.

In our application, the comparator inputs can go high or low over a relatively wide range with respect to the supply voltage (V_{DD}). So, the comparator should be able to respond properly at any value within this wide input range. One of the effective ways is to combine the advantages of N-diff topology and P-diff topology in one composite topology. This topology is called "PMOS/NMOS composite topology" and the input range becomes a

"Rail-to-Rail". Fig. 3-26 shows the schematic circuit of a folded-cascode PMOS/NMOS composite comparator.

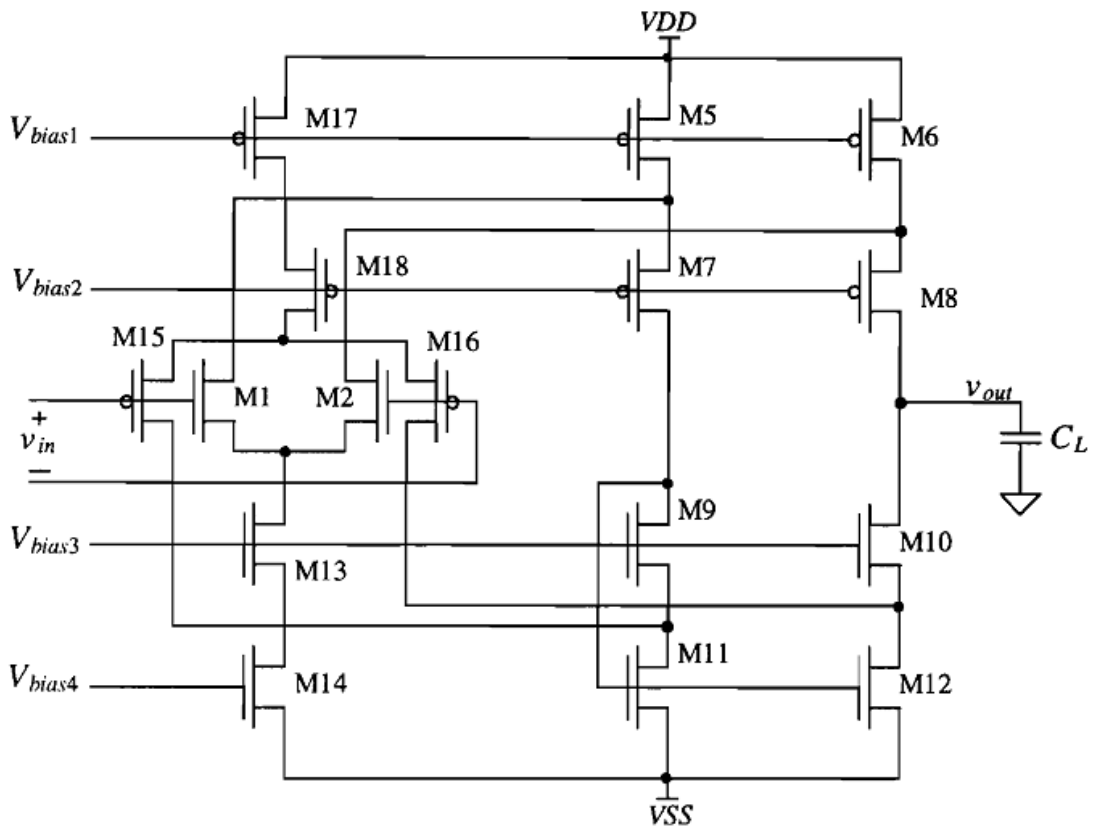


Figure 3-26: Wide-swing folded-cascade comparator topology [43].

The shown topology is consisting of a PMOS folded-cascode Op Amp combined with an NMOS folded-cascode Op Amp. The circuit is designed and simulated. The simulation results of AC response with supply and temperature variation is shown in Fig. 3-27. For testing purpose, a triangular signal and two different error signals are applied to the comparator and the comparator response is tested and verified. The response of the designed comparator is shown in Fig. 3-28.

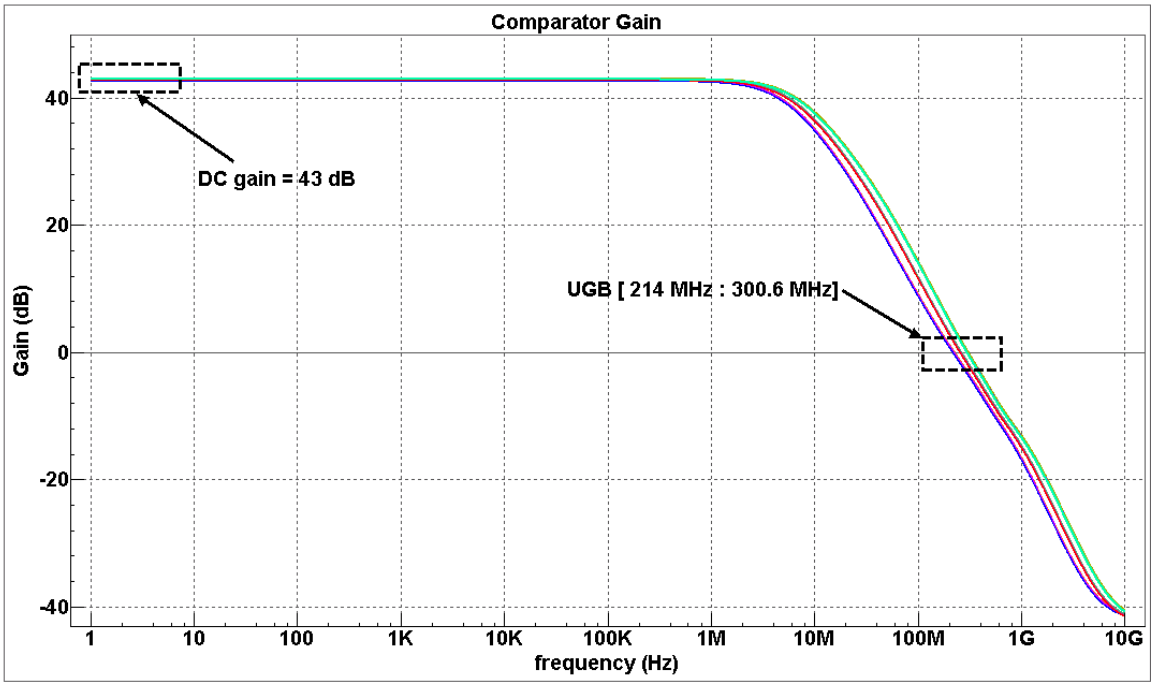


Figure 3-27: PMOS/NMOS folded-cascode comparator gain with supply [±10%] and temperature [-40, 25 and 125 C] variations.

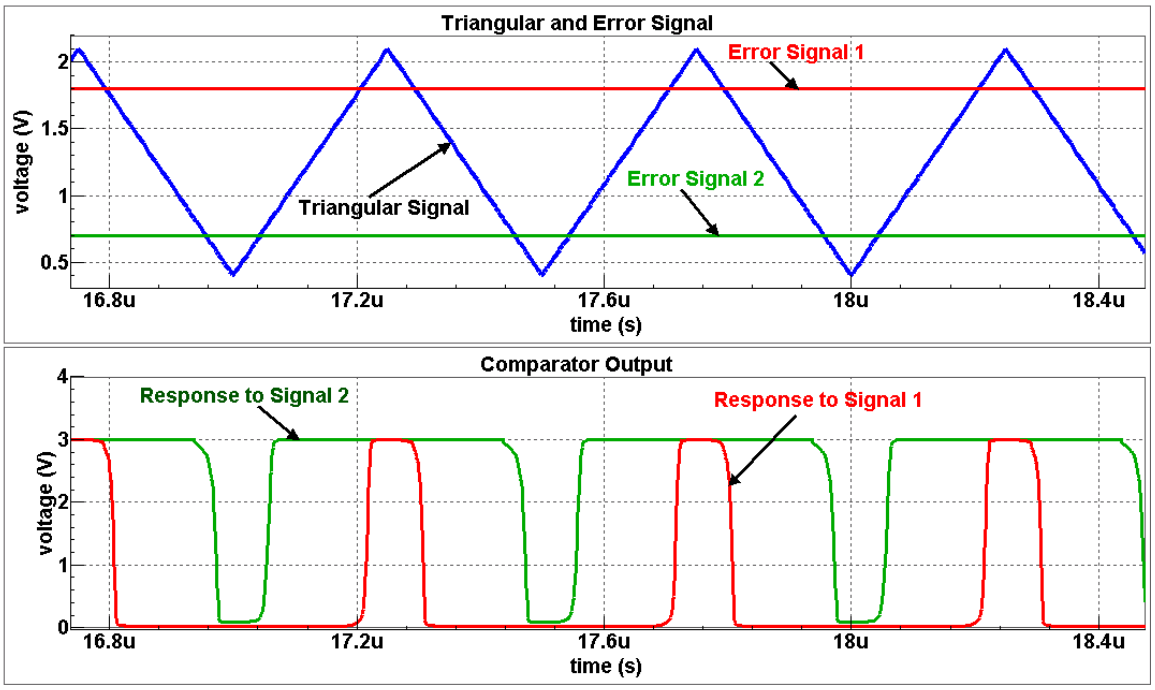


Figure 3-28: Simulation results of comparator response to different error signals.

3.11 Design of Reference Voltage Circuit

Reference voltage circuits are very important block that is needed in most of ICs. In our system as an example, the reference voltage that is applied to the error amplifier is a critical point that affects the operation of PWM control and the whole system. This means that if some changes happened in that reference voltage, the buck output would be respond in a faulty manner. So, this reference voltage should be like an ideal voltage source.

The reference voltage circuit can be defined as a circuit that produces a fixed voltage irrespective of the loading on the device, power supply variations, temperature changes, and process variations. Eliminating the reference variations with respect to other parameters variations is impossible. We can only keep the variation of the reference voltage within an acceptable range.

Bandgap voltage reference is one of the most widely used circuits for generating a fixed reference voltage that is independent on temperature variations. The operation of bandgap circuit depends on adding a voltage that has positive temperature coefficient to a voltage that has negative temperature coefficient. The voltage that has positive temperature coefficient is said to be *proportional to absolute temperature* or PTAT. The voltage that has negative temperature coefficient is said to be complementary to absolute temperature or CTAT. The thermal voltage V_T is an example for positive temperature coefficient and the diode forward voltage is an example for negative temperature coefficient. If these opposite temperature coefficients are combined together in a bandgap circuit, the reference voltage would be

independent of temperature variation. Fig. 3-29 shows the methodology of bandgap circuits.

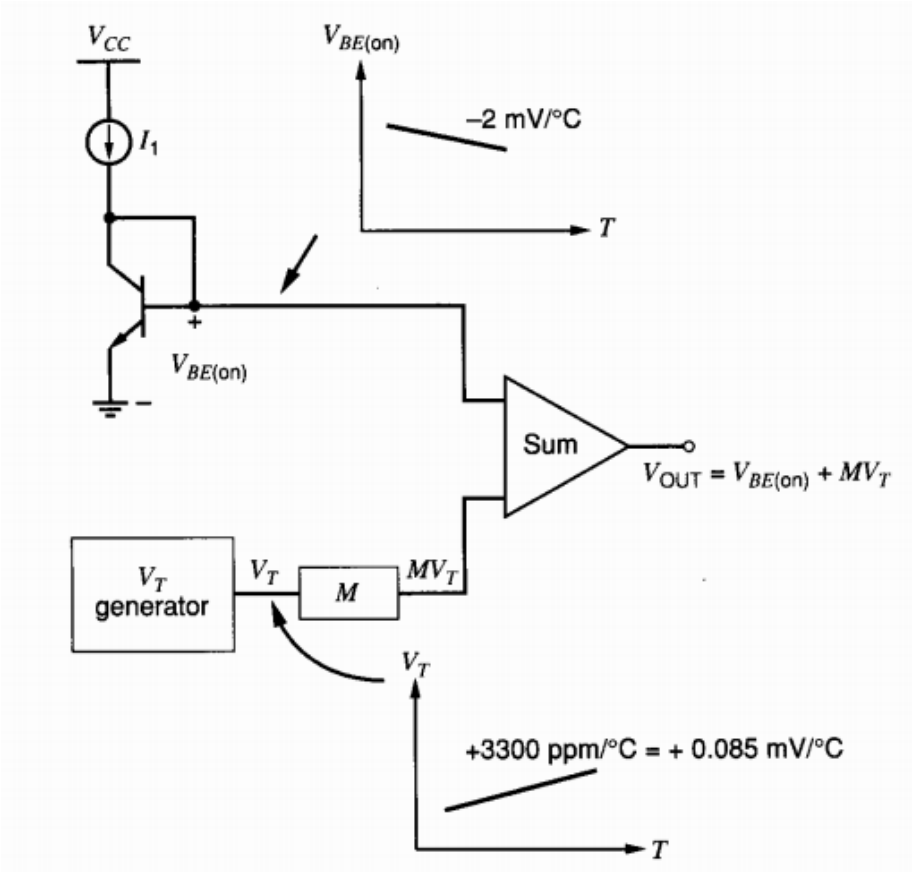


Figure 3-29: Methodology of bandgap reference voltage circuit [44].

Normally, the diode forward voltage is obtained in the form parasitic diode of a bipolar junction transistor BJT. If the base and collector of the BJT are tied together, the BJT is said to be connected as a diode. Sometimes in CMOS process there is no bipolar transistor and a parasitic PNP transistor can implemented instead. This parasitic transistor can be formed by P+ implant as the emitter (E), n-well as the base (B), and p-type substrate as the collector (C). Fig. 3-30 shows the cross-sectional view of parasitic PNP transistor in an n-well CMOS process.

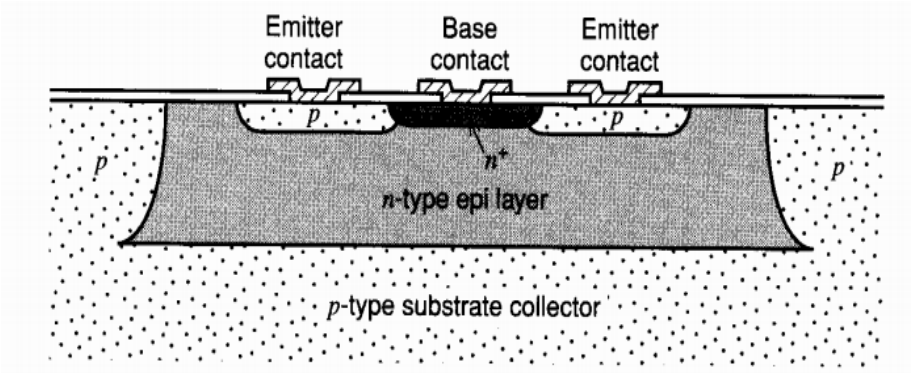


Figure 3-30: Structure of substrate PNP transistor in n-well CMOS process [44].

The negative temperature coefficient of the diode referenced circuit can be combined with the positive temperature coefficient of thermal voltage to form a bandgap reference voltage that is insensitive for temperature. Fig. 3-31 shows a bandgap reference voltage circuit.

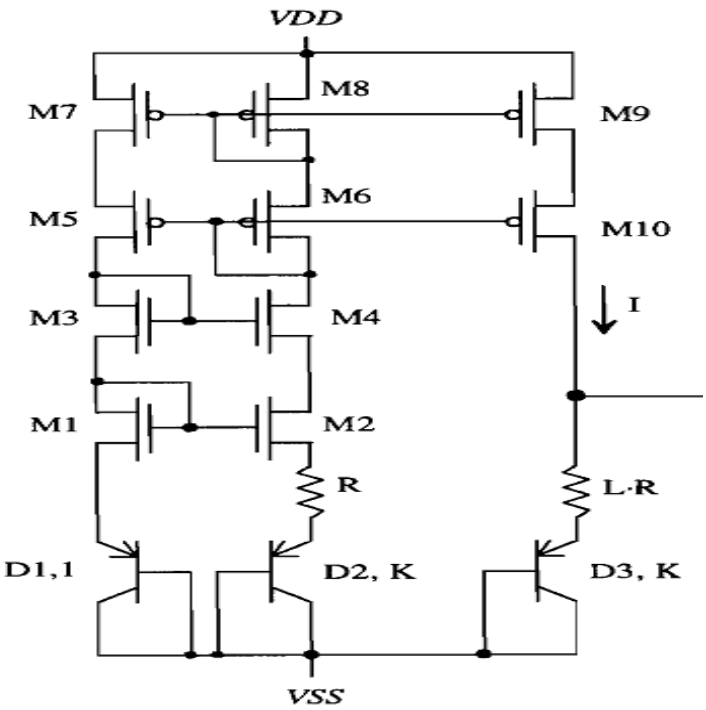


Figure 3-31: A bandgap reference voltage circuit [43].

From the Fig. 3-31, the output voltage of the circuit can be given as:

$$V_{ref} = I\,L\,R + V_{EB3} \qquad (3\text{-}41)$$

In Eq. (3-41), the first term is dependent on the current *I* which is the PTAT component. The second term V_{EB3} represents the CTAT component. By proper design for Eq. (3-41), a reference voltage that is independent on temperature can be obtained.

The circuit in Fig. 3-32 is designed and simulated at temperature sweep from -40°C to 140°C. Also the circuit is simulated at ±10% variation in supply voltage and process variations. The results clarify that the bandgap output voltage has a maximum variation of 17.8 mV over all cases.

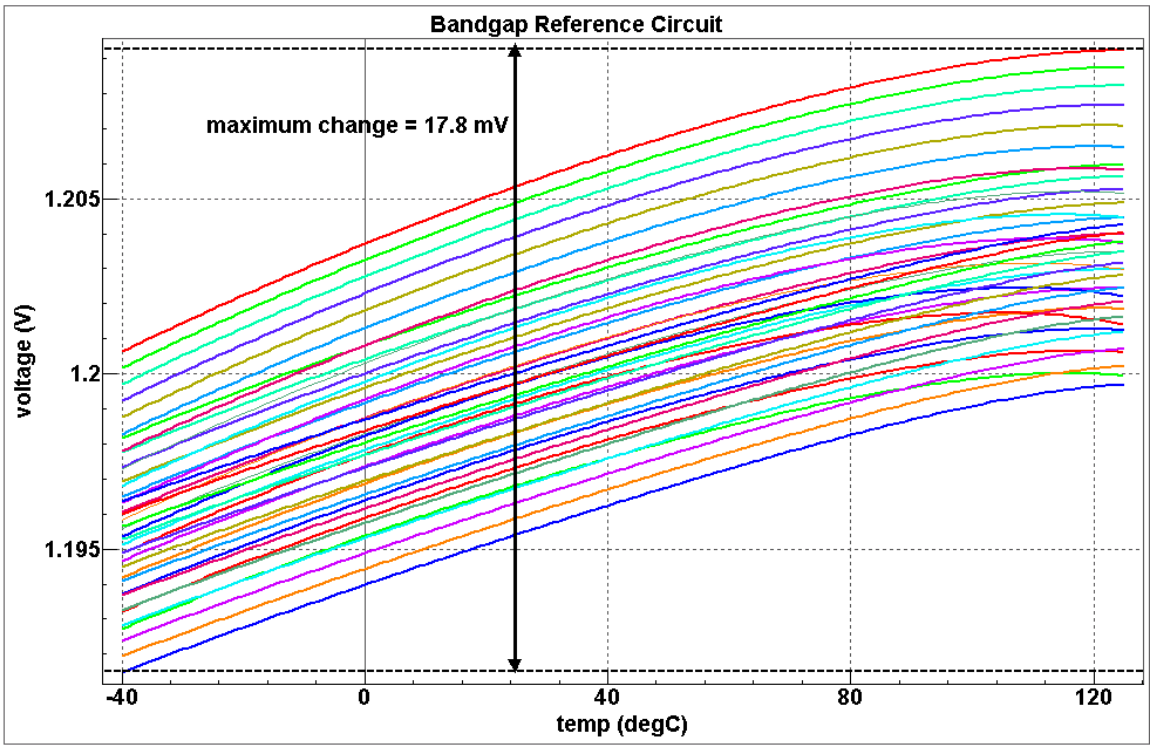


Figure 3-32: The output voltage of designed bandgap with temperature sweep [-40°C:125°C], ±10% change in supply voltage, and process variations

3.12 Design of Supply Voltage Generator

All the controller circuits that are required for buck control and operation are powered from a supply voltage V_{DD}. This voltage supplier is required to be constant and steady at the nominal supply value that is required by the CMOS process. Whatever the input voltage for the buck converter, the supply voltage should be constant. Linear regulator is used to obtain the supply voltage that is required for all the buck converter sub-blocks. Fig. 3-33 shows the simple circuit for linear regulator.

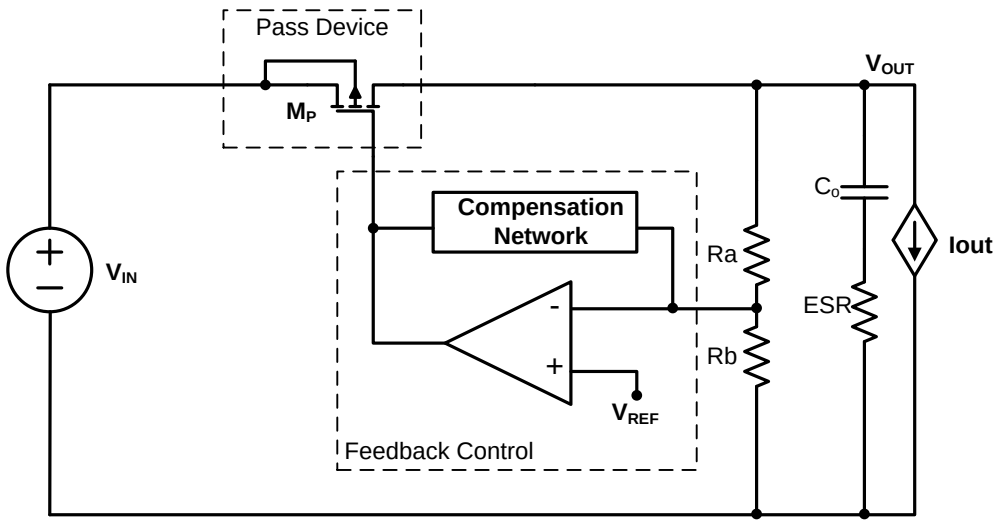


Figure 3-33: Simplified circuit for linear regulator.

The operation of the circuit depends on controlling the on-resistance of pass device until the required output voltage is obtained. Simply, the pass device can be considered as a voltage-controlled current source that is controlled by the voltage applied by the Op Amp. The Op Amp has the role of monitoring the output voltage by comparing it with a fixed reference voltage. If the output voltage decreased, the Op Amp output will decrease (in the case of using PMOS as pass device) to decrease the on-resistance of pass

device. In the case of increased output voltage, the Op Amp output will increase to compensate for this change and so on. The compensation network has the same role as any compensation in any closed loop control. It has the role of stabilizing the system under all conditions.

The input voltage for linear regulator is the input voltage for buck converter which equal 3 V. The linear regulator should produce a constant 2.5 V like what is required by all the controller sub-blocks. The linear regulator circuit is designed to work at maximum output current of 6mA. Fig. 3-34 shows the simulation result for the linear regulator at load change from 1 mA to 5 mA. As shown, undershoot and overshoot percentages at the output voltage is in the range of ±12%. These percentages are relatively high, however the change of output current from 1 mA to 5 mA in high slew rate is considered as the worst case. The response of the linear regulator is still sufficient and acceptable.

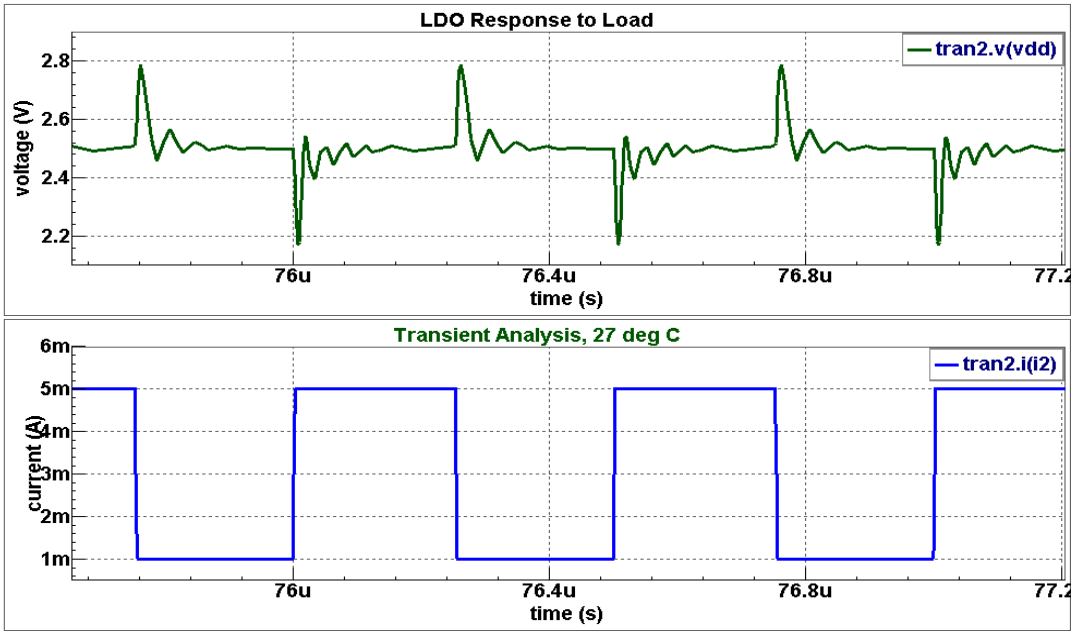


Figure 3-34: Linear regulator response to output current change.

3.13 System Integration and Simulation Results

After finishing the design of the controller sub-blocks shown in Fig. 3-26, the system is integrated and the buck converter with its sub-blocks is simulated.

The most important waveforms for the designed buck converter are shown in Fig. 3-35. The first subplot shows the inductor current at full-load (10 A). The second subplot shows the triangular signal and the error signal which are compared to each other. The switching node voltage in a response to the error signal is clearly shown in the third subplot. The switching voltage is filtered to produce the output voltage of the buck. The output voltage of the buck is shown in the fourth subplot. The output voltage has 13 mV peak-to-peak ripples. The ripple percentage is 1.3% which smaller than the target of 3%. Of course, smaller output capacitor can be used to achieve the target and minimize the PCB area of the capacitor.

The load transient response of the designed buck converter is shown in Fig. 3-36. The buck converter response is tested by applying an output current pulse from no-load (0 A) to full-load (10 A) with slew rate 0.1A/ns. Undershoot and overshoot percentages is less than 15% as shown in the figure.

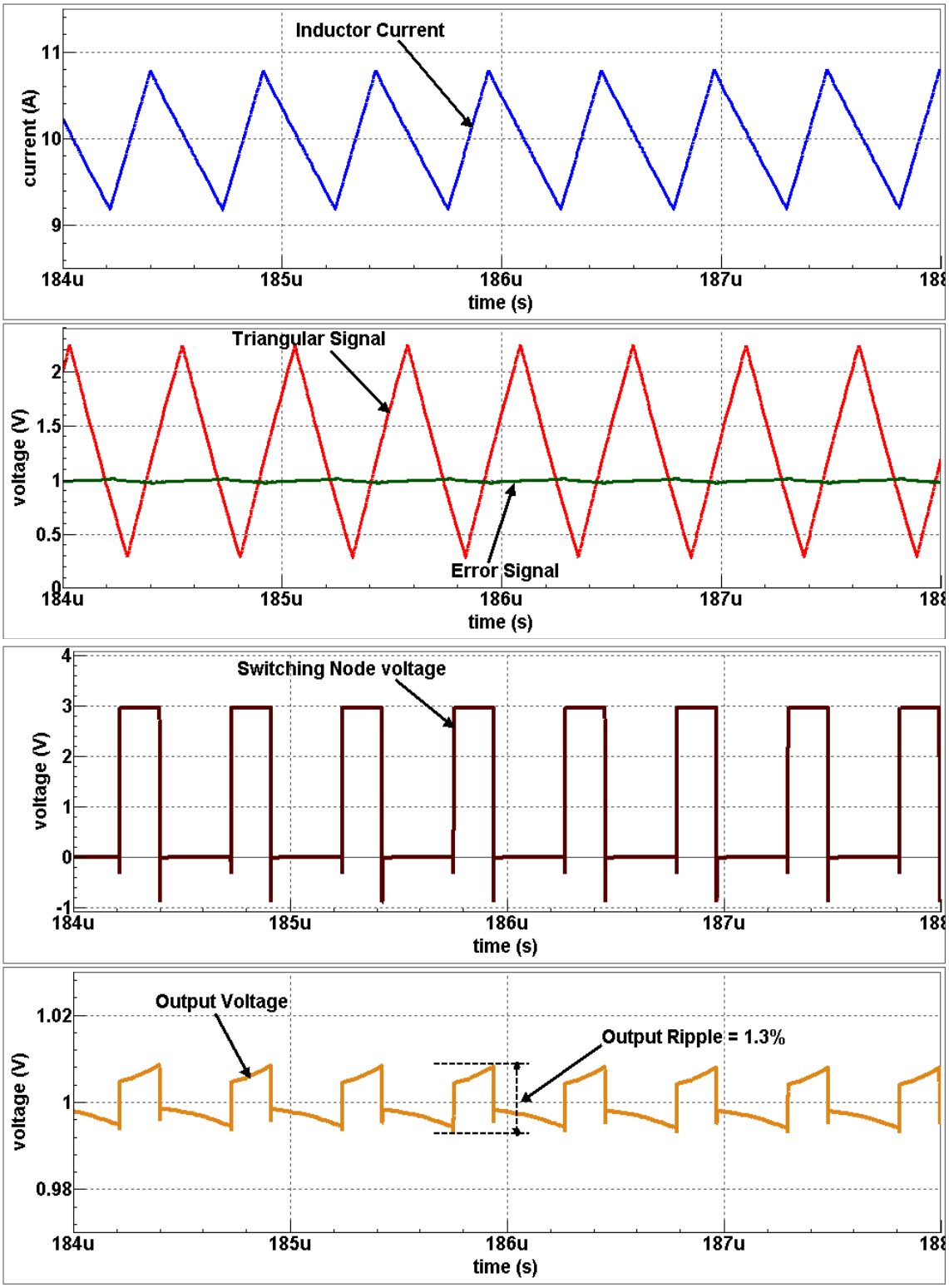


Figure 3-35: Most important waveforms in the buck converter.

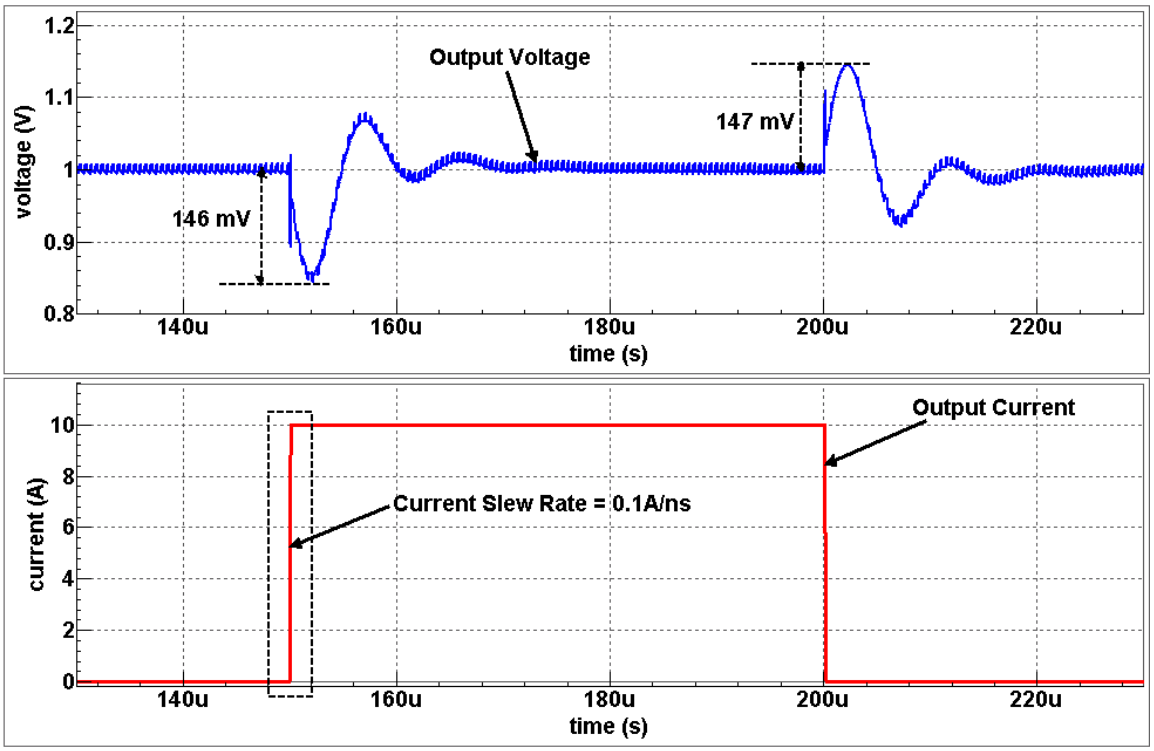


Figure 3-36: The load transient response of the designed buck converter

(V_{IN} = 3V and V_{OUT} = 1V).

3.14 Experimental Results

The proposed system has been fabricated using a 0.25 µm CMOS technology. The experimental setup is shown in Fig. 3-37.

The high-side MOSFET gate signal and switching node voltage waveforms are shown in Fig. 3-38a and Fig. 3-38b at 0 A and 10 A consequently.

Figures 3-39a and 3-40b show the output voltage ripple at 0 A and 10 A consequently. The first subplot of each figure shows a measurement with limiting the bandwidth of the oscilloscope to 20 MHz and the second subplot shows the ripple in a full oscilloscope bandwidth (100 MHz). The figures show that the output ripple is less than 20 mV peat-to-peak.

Finally, the experimental efficiency is shown in Fig. 3-40. The resulting efficiency exceeds 91% at full-load (10 A) and has a maximum value of 93.5% at 5 A.

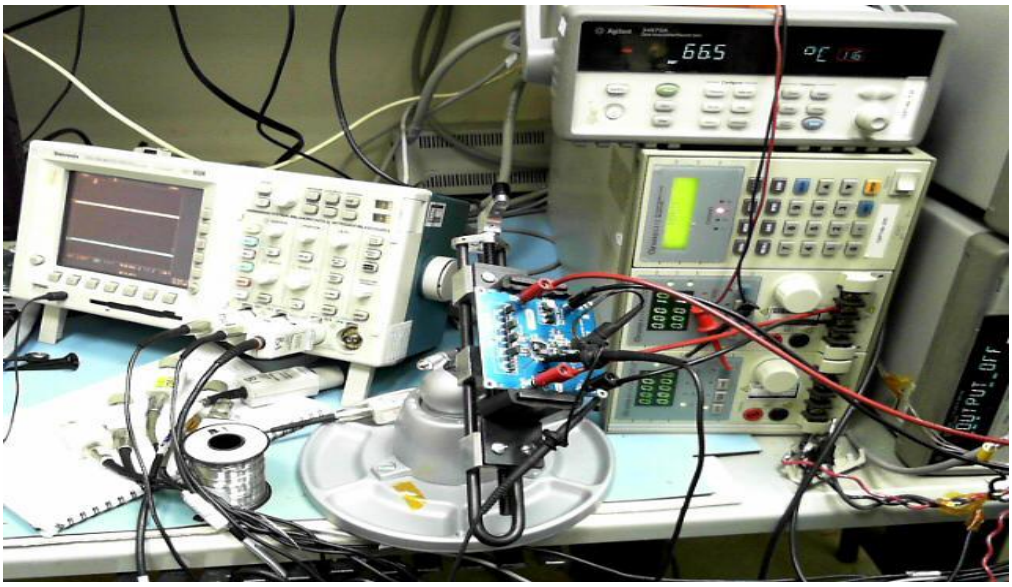
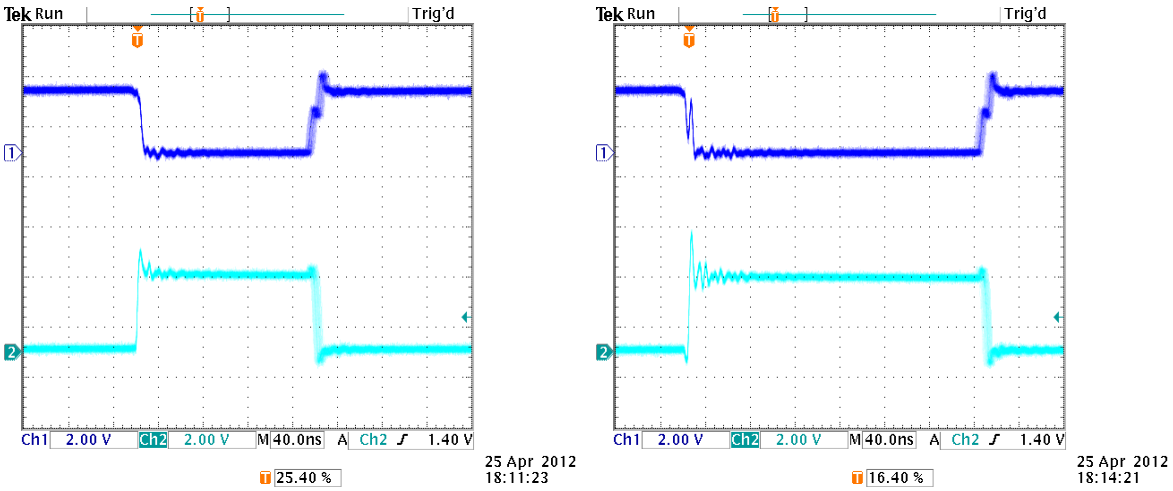
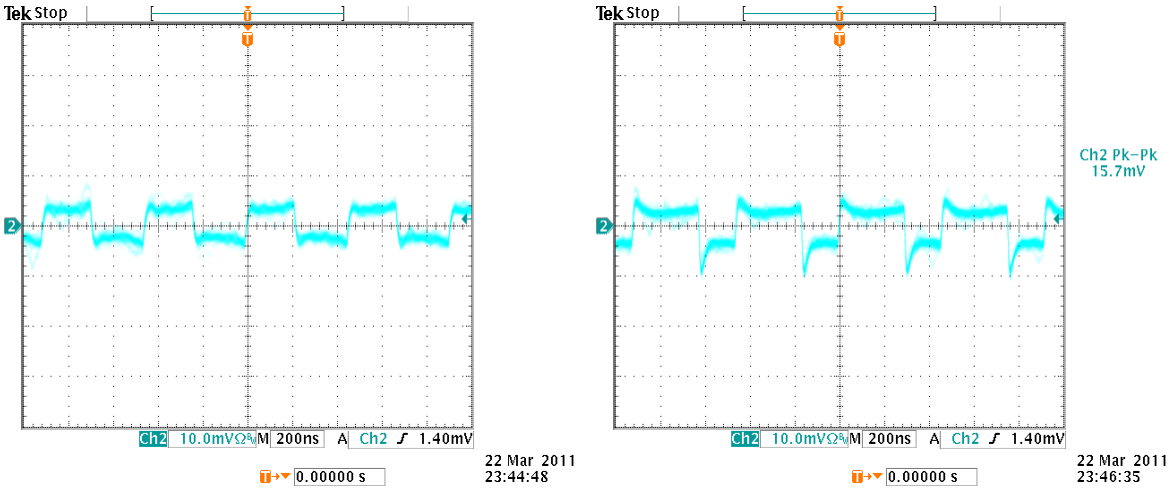


Figure 3-37: Experimental setup of fabricated IC.



(a) I_{LOAD}= 0 A (b) I_{LOAD}= 10 A

Figure.3-38: PFET gate voltage on Ch1 and switching node voltage on Ch2.



(a) I_{LOAD}= 0 A (b) I_{LOAD}= 10 A

Figure.3-39: Output voltage ripple at no-load and full-load.

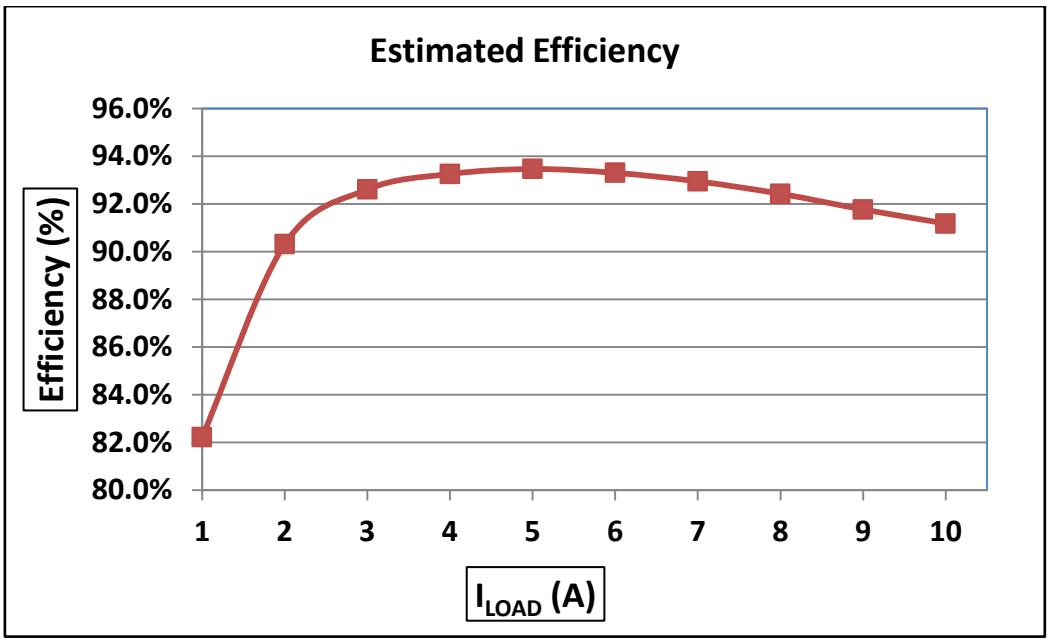


Figure 3-40: Efficiency of designed buck converter.

3.15 Conclusion

In this chapter, the operation theory of buck converter is discussed. The design procedures of the buck converter power-stage are described in details. The PWM control is discussed and its sub-circuits are designed separately. The design of 2 MHz buck converter to be the second stage of our DC-DC converter is done in details. The buck converter circuits are integrated and tested. The simulation results show that the converter has small output ripple and tight regulation in addition to high efficiency at full-load exceeding 91%.

Chapter 4

Integrated Two-Stage Power Supply

Chapter 4

Integrated Two-Stage Power Supply Design

4.1 Introduction

There are many well know types of DC-DC converters which fit certain applications. The different types of DC-DC converters were described briefly at the previous chapter. The selection between the different types depend on the key parameters of the power supply, which are cost, overall size, EM performance, noise and efficiency.

The importance of each parameter varies between the application and trade-offs made between each of them. For example, a solution targeting the lowest cost may be quite different from one targeting the highest efficiency; counter-intuitively a solution targeting the highest power density (smallest size) won't necessarily achieve the lowest losses [13].

For our application, the processor's core voltage is smaller than 1.0 V which mean that we need a buck-mode converter or buck switching regulator. Synchronous buck converter is a brilliant choice for low-power processor application. However, synchronous buck converter has some limitations which need to be solved.

In this chapter, the limitations of buck converter will be mentioned. To solve these limitations, a new power architecture composed of two stages will be developed. The advantages of the two-stage power supply will be discussed followed by the design of the system. The two-stage system will be realized by integrating the SCC and buck converter that have been designed at chapters two and three. The simulation results of the two-stage power supply will be shown followed by a comparison with the conventional one-stage conversion at the end of this chapter.

4.2 Limitations of Buck Converter

The buck circuit is in widespread use to provide high current, low voltage supply for microprocessors. But as the buck input voltage increases and lower output voltages are required, the buck converter may fail to meet the target of high efficiency as the operating duty cycle becomes small. The small duty-cycle will significantly reduce the power supply efficiency and slow down the transient response, and potentially may cause the malfunction of the power supply under high frequency operation because of small conduction time for top switches [15].

So, if we decrease the input voltage for the buck converter we can achieve the following advantages:

- Higher efficiency due to the increase in duty cycle and the decrease in switching loss.
- The ability to use low-voltage (LV) switches which effectively decrease the solution footprint and exhibit lower on-resistance.
- Reduce the fabrication cost as the LV switches save the cost of the additional fabrication masks required by HV switches.

In [16] a two-stage approach for 12 V power supply is proposed. The idea of that approach is to solve the small duty cycle problem by dividing the system into two stages. The authors designed their system for laptops power supply and for very high output current (100 A), and they reviewed their idea by implementing a test prototype. However, the authors in [16] predicted that the two-stage approach will open the window for advanced integration

and packaging of the system. So, our proposed idea depends on this prediction.

Our proposed idea is to replace the conventional one-stage power supply by the two-stage VR even for LV regulators. The LV regulators enable us to integrate the two-stage at the same package which give us advantage at size, cost and efficiency.

4.3 Proposed Power Architecture

In the mid-80s Bell Northern Research coined the phrase "point of use power supply" (PUPS) for the modular DC-DC converters or bricks on line cards in telephone exchanges. This Distributed Power Architecture is shown in Fig. 4-1 [17].

As the required number of power supply rails on the system card increased due to complex load circuitry system designers turned to the Intermediate Bus Architecture (IBA). This technique is shown in Fig. 4-2.

As CMOS technology offers the power management IC designer increased current density and sophisticated control, steps are being taken to reduce the intermediate bus potential to below 6 V, the breakdown voltage of 5 V CMOS processes [17].

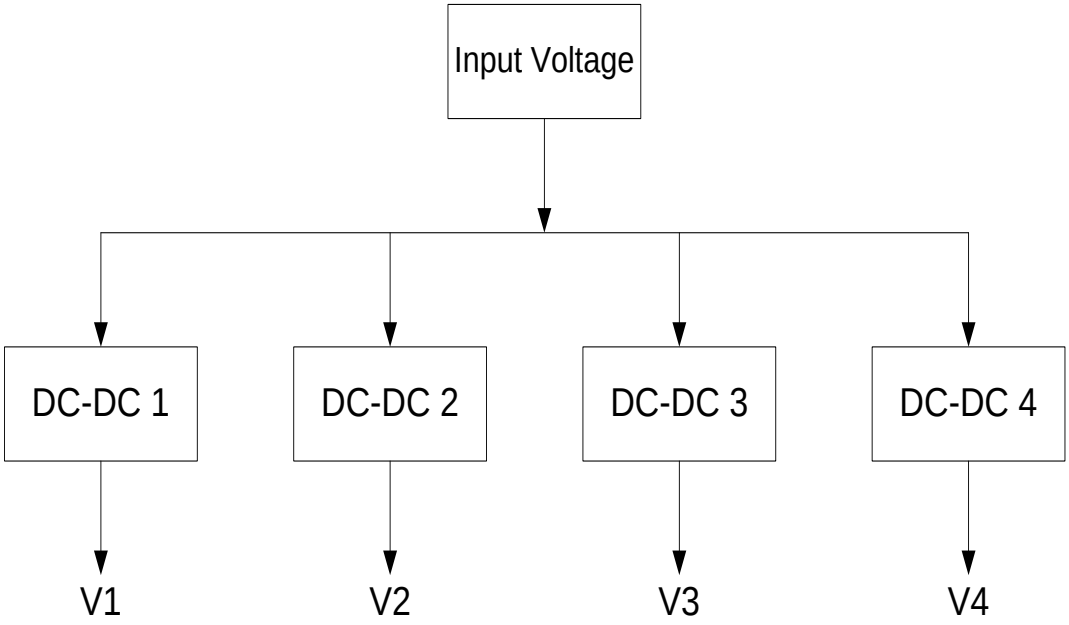


Figure 4-1: Classic distributed power architecture [17].

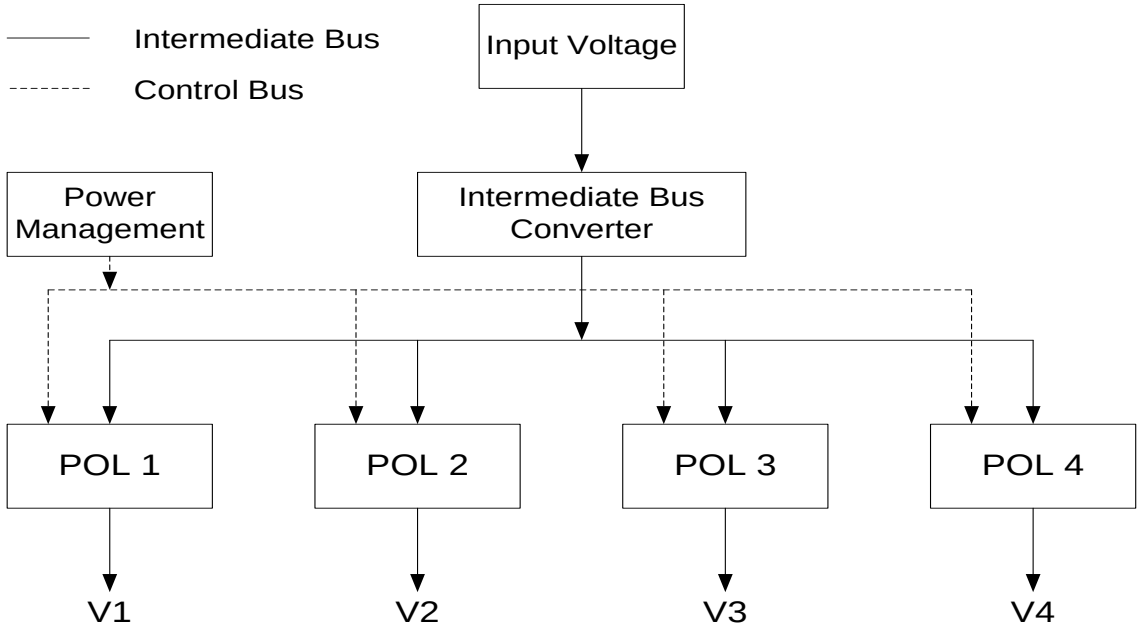


Figure 4-2: Intermediate bus power architecture [17].

Previous design of LV 6V power supply is the conventional one-stage buck converter. Our proposed idea is to apply the two-system for LV power supplies as well. LV regulators allow us to integrate the power switches, controller, and protection circuit in one package. Adopting the two-stage system architecture at the design of LV regulators enable us to integrated the two-stage at one package which will give us advantage at both size and efficiency. Our proposed architecture is to divide the LV converter from 6 V to 1 V into two stages as well. So, the 12 V power supply can be as shown in Fig. 4-3.

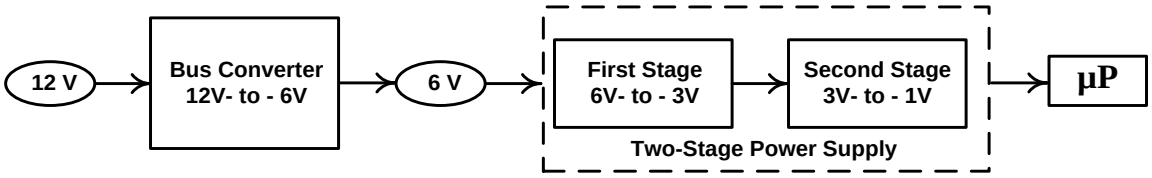


Figure 4-3: Proposed power architecture for 12 V VRMs.

In [18] the second stage is multi-phase buck converter with input voltage 6 V. Our proposed idea is to divide the second stage into two-stages. So the 12 V VRMs will be reached through three stages instead of the architecture in [18]. Our idea is not directed only toward dividing the LV VRMs in two-stage, but in integrating the two-stage on one package.

In [18] the efficiency of SCC is compared with buck converter, and SCC give advantage at both size and efficiency. The requirement of the second stage is to be simple, efficient, and smaller in footprint. Generally, SCC is the best choice for the second stage at all. Switched capacitor converter has the following advantages:

- High power density.
- It can be optimized for high efficiency.
- It is inductor-less which reduces the problem of radiated EMI.

The target of the second stage is to produce the regulated output voltage for the microprocessor. So, for the LV two-stage power supply, the task of regulation is the responsibility of the buck converter adopted in the second stage. There is no need for the SCC to be regulated.

The proposed architecture of our 6 V power supply is shown in Fig 4-4.

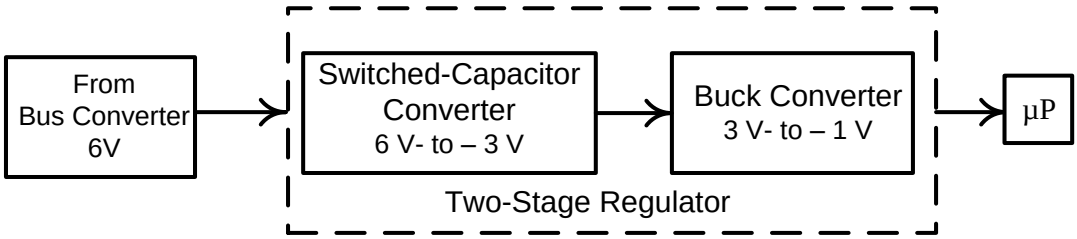


Figure 4-4: Proposed two-stage architecture for 6 V power supplies.

Conventional trend in the design of microprocessors power supply is to receive the bus converter output (5 V – 6 V) and apply it directly to one-stage buck converter. This buck converter converts from the bus converter voltage to the microprocessor voltage. Due to the limitations of buck converter duty cycle, the conversion process will be split into two stages. The first stage will adopt the SCC that has been discussed and designed in chapter two. The SCC will receive the bus voltage (has worst case value of 6 V) and divide it by two which yields approximately 3 V. The second stage will adopt the buck converter topology which receives a lower input voltage. The efficiency of buck converter will be greatly enhanced as its input voltage will be lower.

4.4 Market Examples

A lot of commercial products for powering the microprocessors are available in the market. All these commercial products meet the latest power needs for Intel Atom processors.

Due to its superior performance and the best efficiency/solution size mixture, Enpirion's EN5395 will be taken as the first market example to be compared with the two-stage power supply.

Fig. 4-5 shows the functional block diagram of EN5395. The converter integrates the inductor, MOSFETs, and controller in a single tiny package.

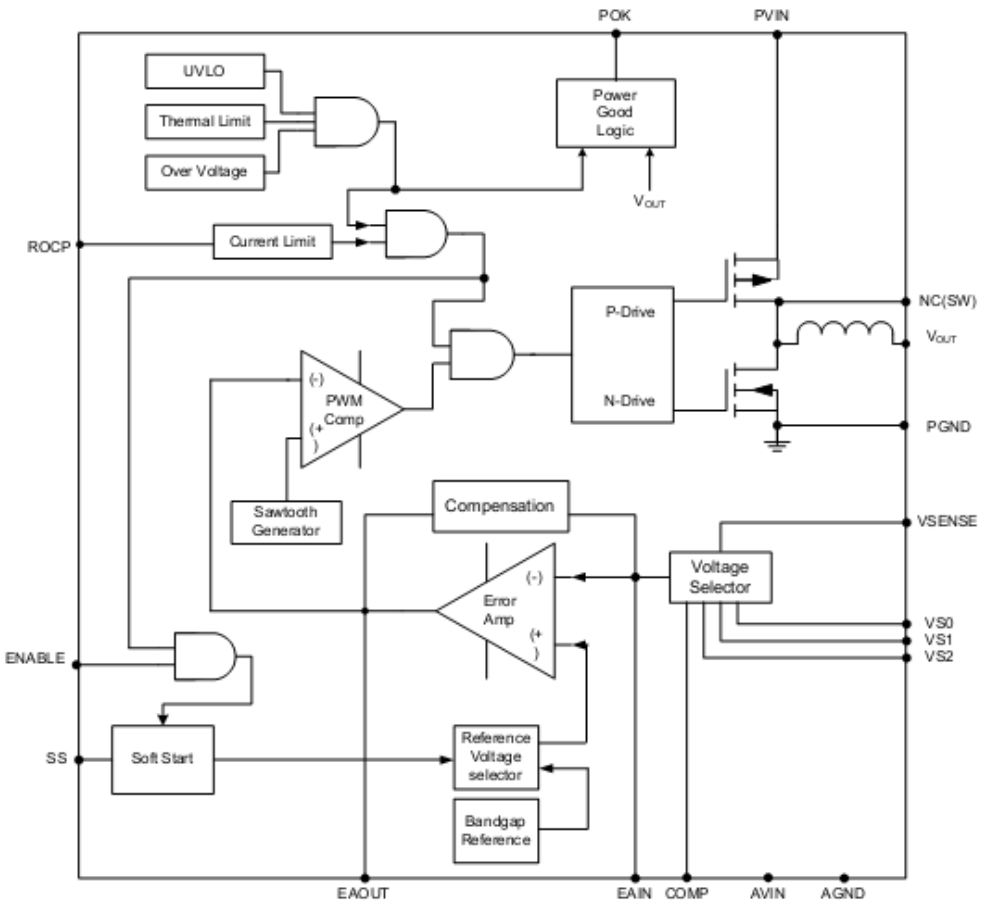
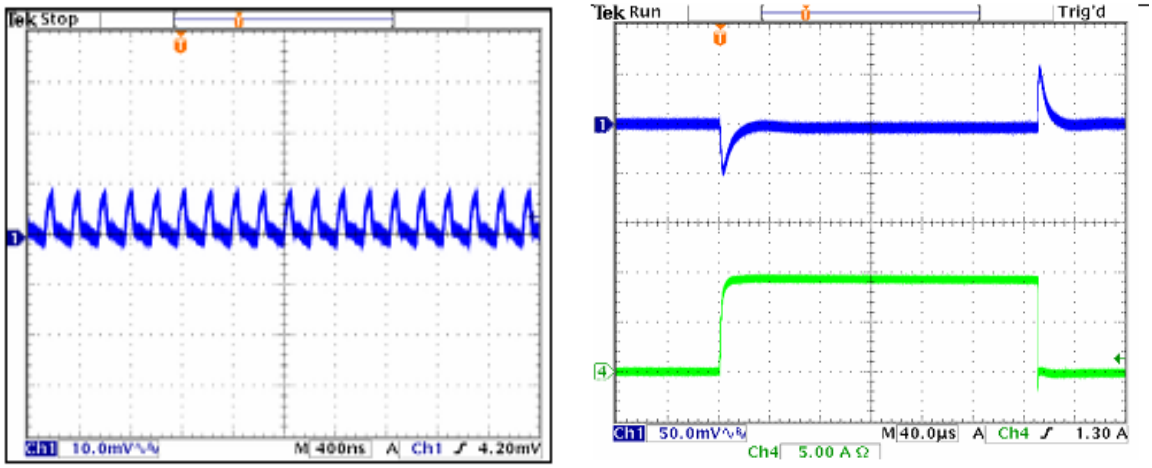


Figure 4-5: Functional block diagram of EN5395 [27].

The converter operates on a single switching frequency of 5 MHz, and the power stage utilizes a P-channel and N-channel power MOSFETs. EN5395 IC can operate with input voltage range from 2.375 V to 5.5 V. The output voltage is programmed using an external resistor divider network or using 3-Pin VID output voltage selector. The control loop is voltage-mode with a type III compensation network. Much of the compensation circuitry is integrated in the device.

The ripple and load transient response of EN5395 is shown in Fig. 4-6. The figures show about 10 mV (less than 1%) peak-to-peak of output voltage ripple and about 55 mV (less than 5%) undershoot and overshoot due to load transient from 0 to 9 A.



(a) Output ripple at 5.5 Vin/1.2 Vout, I_{OUT}=9 A, C_{OUT}= 5x22uF.

(b) The load transient response of EN5395. Ch.1: V_{OUT}, Ch.4: I_{LOAD} (slew rate = 7A/µS) and C_{OUT} = 5x22µF

Figure 4-6: Ripple and load transient of EN5395 [27].

The second market example is Maxim MAX15112. This product is a high efficiency 12 A step-down regulator with integrated switches. The MAX15112 offers excel-lent efficiency with skip mode capability at light-load conditions. A factory-trimmed switching frequency of 1 MHz (PWM operation) allows for a compact, all-ceramic capacitor design.

Fig. 4-7 shows the functional block diagram of MAX15112. The converter integrates the MOSFETs and controller in a single chip.

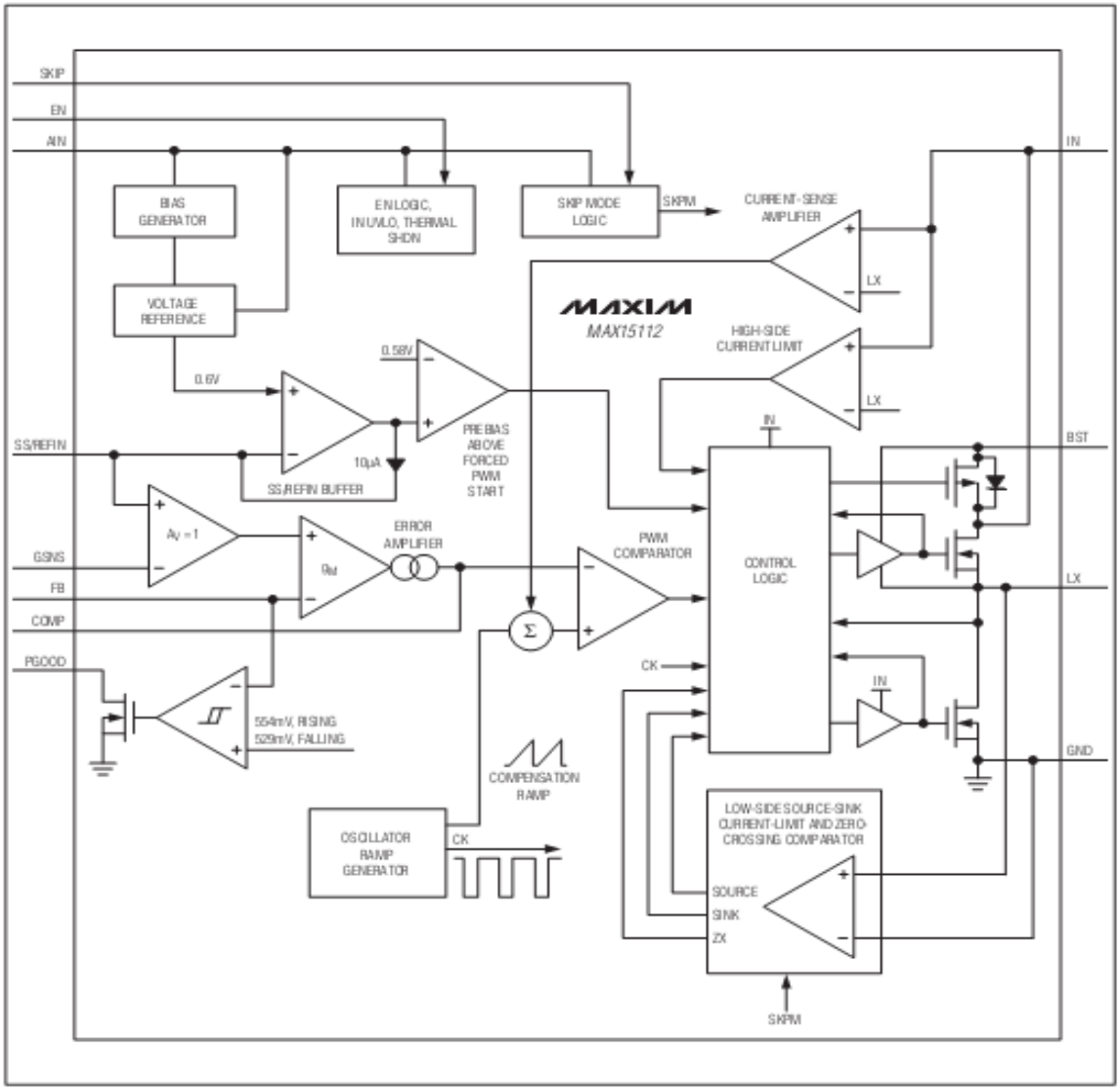


Figure 4-7: Functional block diagram of MAX15112 [Ref].

4.5 Integration of The Two-Stage System

The two-stage system that has been described in Fig. 4-4 is integrated and simulated. The integration is done using the SCC that has been designed in chapter two and the buck converter that has been designed in chapter three.

Fig. 4-8 shows the no-load output voltage of each stage after connecting them together. The first subplot shows the output voltage of SCC and the second subplot shows the output voltage of the buck converter.

Fig. 4-9 shows the full-load output voltage of each stage. In the first subplot, it is noted that the output voltage of SCC drops to an average value of 2.86 V because there is no regulation in the SCC. In the second subplot, the output voltage of buck converter is still the same because of its regulation behavior.

Fig. 4-10 shows the behavior of the two-stage system as a response to sudden load change from 0 A to 10 A with a slew rate of 0.1 A/ns. The first subplot shows the output voltage of SCC. The second subplot shows the output voltage of buck converter. The third subplot shows the output current of the system. The figure shows a 14.7% undershoot and 14.6% overshoot. The load transient response is tested with two 47 µF output capacitor without the use of the proposed linear-nonlinear control.

Fig. 4-11 shows the two-stage efficiency vs. load current. The resulting efficiency exceeds 87% at full-load and has a maximum value of 90.95% at 5 A.

Finally, a comparison between the efficiency of the two-stage system and the conventional one-stage buck converter is shown in Fig. 4-12. This

comparison is done to prove the benefit of the two-stage system from the efficiency point of view. The figure shows that the two-stage system have a better efficiency than the one-stage buck converter by at least 7% at high loads and 12% at light loads.

For more validation for the two-stage benefits, the efficiency of the two-stage converter is compared to the market examples for Vin = 5 V and Vout=1 V. The efficiency comparison is shown in Fig. 4-13. The efficiency curves show that the two-stage converter can be higher than EN5395 by at least 8.5% and higher than MAX15112 by at least 1.6%.

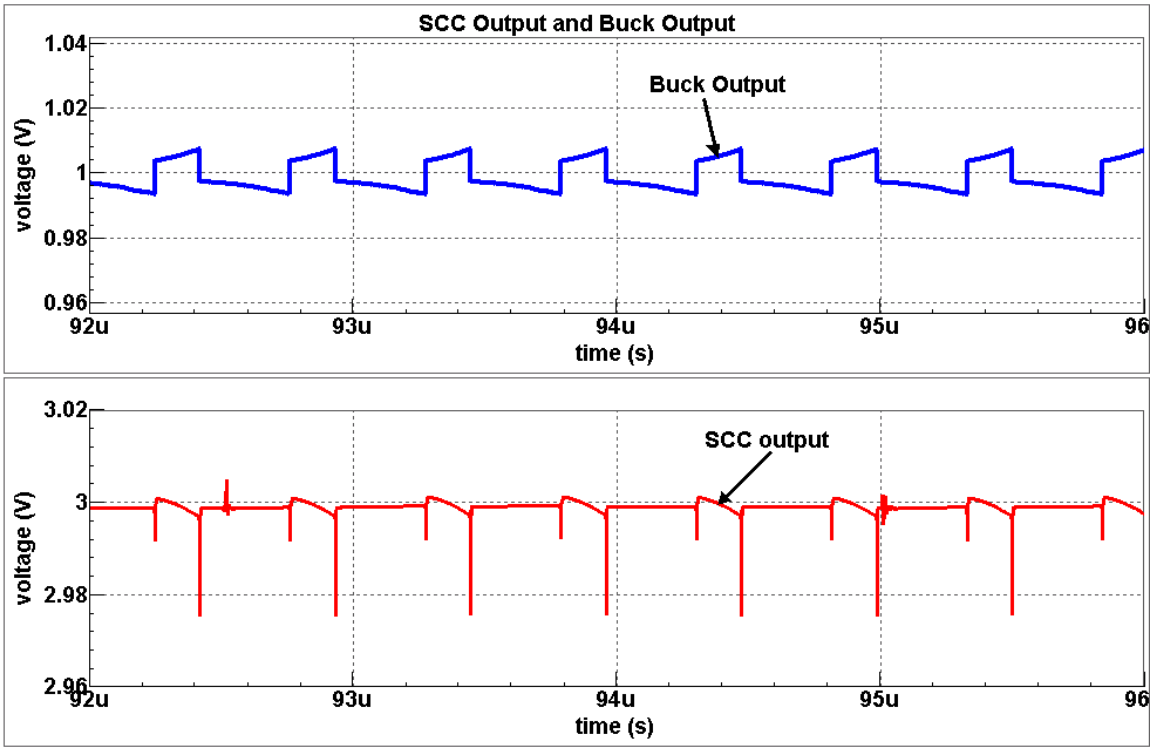


Figure 4-8: SCC's output and buck's output of the two-stage system at no-load.

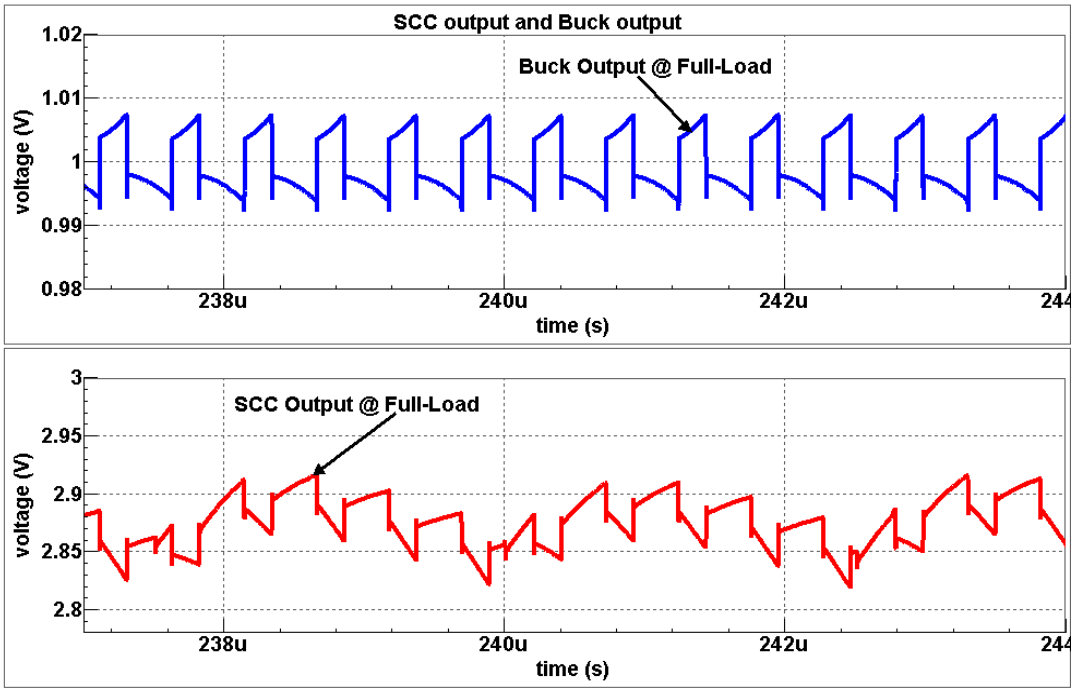


Figure 4-9: SCC's output and buck's output of the tow-stage system at full-load.

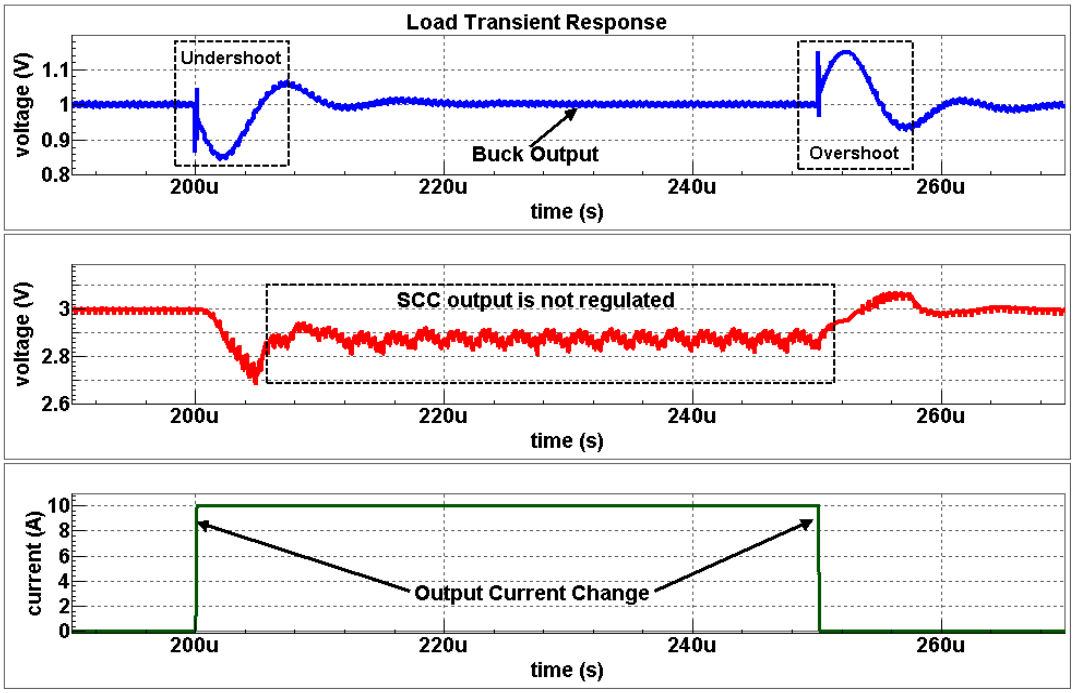


Figure 4-10: Load transient response of the two-stage system.

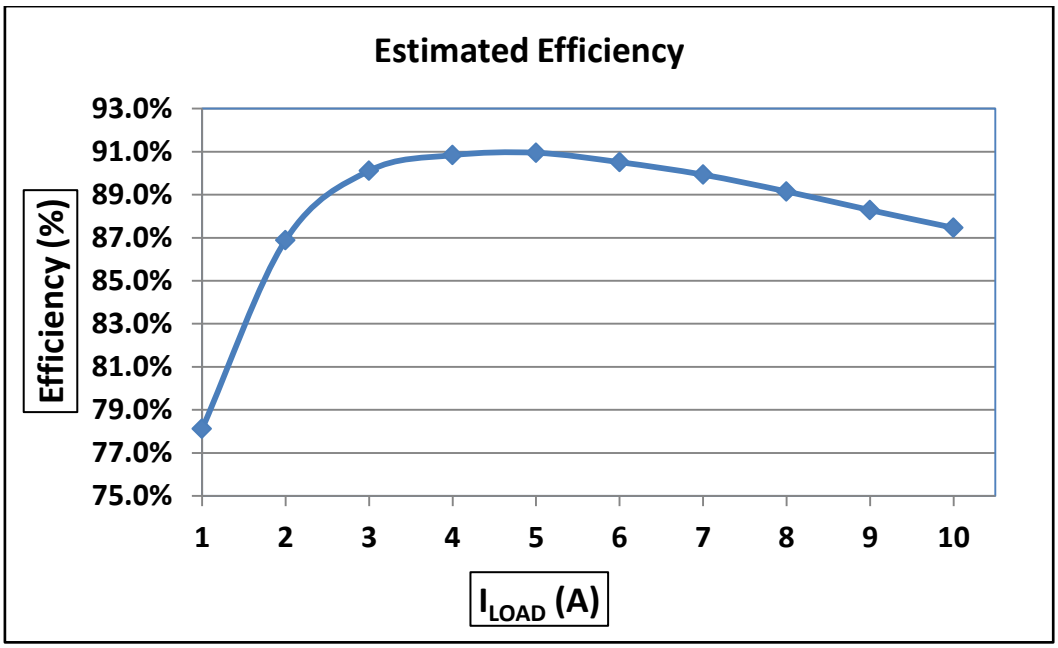


Figure 4-11: Simulated efficiency of the integrated two-stage system.

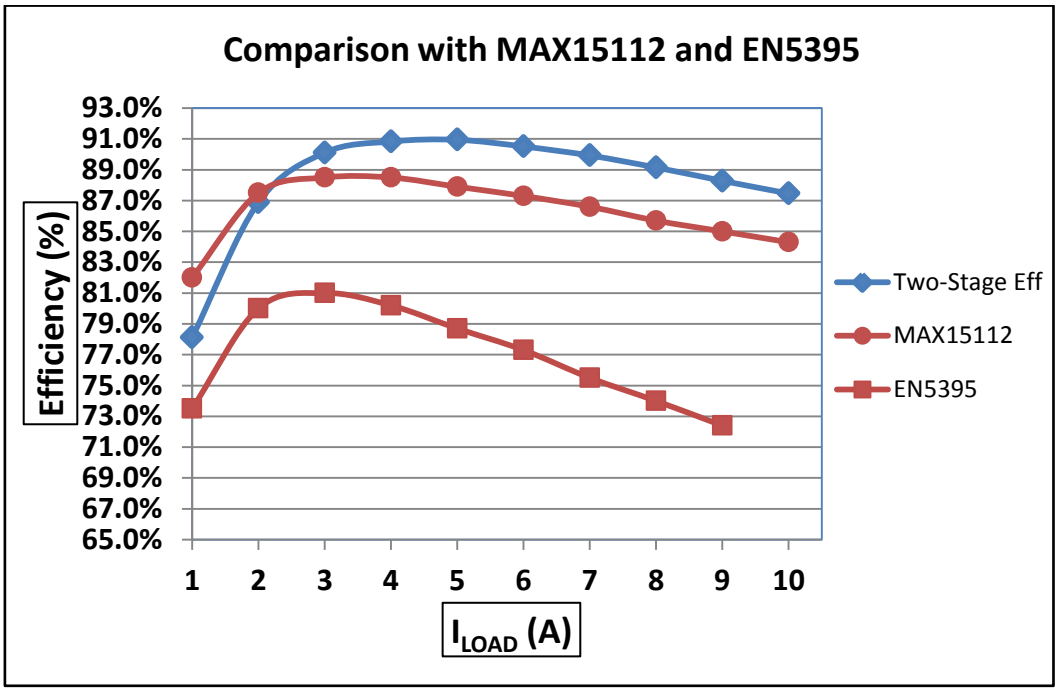


Figure 4-12: Comparison between efficiency of two-stage and efficiency of the two market examples.

4.6 Conclusion

In this chapter, the two-stage power architecture is proposed to be used in the design of microprocessor power supply. The two-stage is originally proposed to solve efficiency limitations of buck converter.

The SCC that is previously designed in chapter two is integrated with the buck converter designed in chapter three to implement the two-stage system. The simulation result of the integrated two-stage system showed that high efficiency can be obtained at high output current. Then, the efficiency of two-stage approach is compared with the two selected market examples. The comparison showed that the two-stage system is higher than EN5395 by at least 8.5% and higher than MAX15112 by at least 1.6%.

Chapter 5

Design of Linear-Nonlinear Control Technique for Buck Converter

Chapter 5

Design of Linear-Nonlinear Control Technique for Buck Converter

5.1 Introduction

Fast transient response is an important requirement for most of the DC-DC converters, especially for portable application since the output voltage is going lower and lower and the tolerance is smaller and smaller [59]. The slow transient response of regulators is not suitable for today's application.

The last stage in our DC-DC converter is the buck regulator. The buck regulator that has been designed in the previous chapter is employing a voltage-mode (VM) control. Since, the basic operation of VM controlled buck converter does not satisfy the fast transient requirement, a lot of researchers worked on how to make the buck converter respond vastly to minimize the output voltage undershoot and overshoot percentages. In [60], a pseudo-type III compensation technique is proposed to improve the response of the voltage-mode control, but this method increases the capacitance area compared to the conventional type III which increase the silicon area if the capacitors are implemented on-chip. In [61], an adaptive on-chip capacitor multiplier is implemented to compensate the error amplifier and speed its

response during transient. This method depends on charging and discharging the error amplifier output capacitor to speed it response, but speeding the error amplifier output cannot help in speeding the buck response as the dynamic response depend on the loop bandwidth and output capacitor value too. In [62, 63], a high performance error amplifier is proposed to increase the error amplifier slew rate to speed the response to load transient. The two methods are good from slew rate point of view but these methods also neglected that even increasing the error slew rate will not be useful if the output capacitor value is small and the loop bandwidth is low. The last methods depend on sensing a scaled version of the output voltage and compare it to low and high threshold levels.

The comparison made always ignore the effect of output voltage ripple. If the output voltage is sensed without taking the effect of ripple into account, this may lead to false triggering of the technique and output instability. Comparing a constant reference voltage to a constant voltage with a ripple on it will make the comparator oscillate by a frequency equal to the frequency of the ripple voltage. Fig. 5-1 shows the comparator output if the scaled output voltage is compared to a constant reference voltage (V_{ref}) directly. It is clear from Fig. 5-1 that the output voltage ripple will make the technique turns on faulty.

Our proposed technique is to combine a nonlinear control technique (NCT) together with the conventional VM linear control. The nonlinear control is off during normal operation of the buck converter and turns on only during any disturbance on the buck converter output. Most of the time, the disturbance at buck output is due to load change.

The nonlinear control technique turns on during output disturbance only. If the NCT is left to operate at any time for a long period of time it may cause instability issue. So, a nonlinear operation monitoring (NOM) system is designed. The NOM system makes sure that the NCT operate well without triggering any instability issue at the buck output.

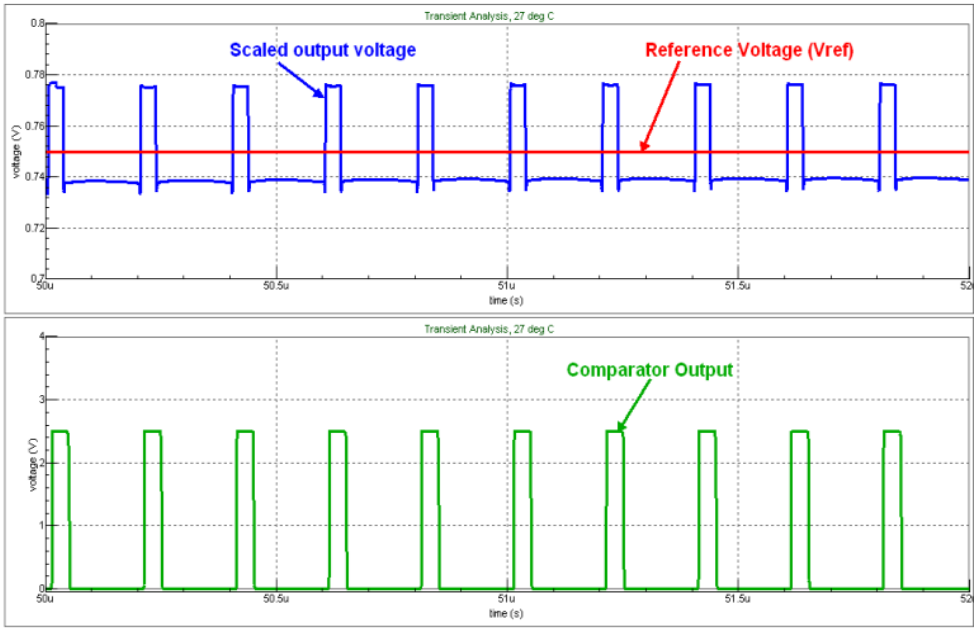


Figure 5-1: Effect of Output Ripple on Comparator Output.

This chapter is organized as follows. The basic idea of the proposed technique is introduced, as well as, the design of NOM system is presented. The testing and simulation results of the system and comparison with the conventional VM linear control are also illustrated for validating the new control. At the end of this chapter, the NCT is integrated in the buck converter of the two-stage system and the overall operation and performance of the system is tested.

5.2 The Proposed Nonlinear Control Technique

In [62], a new error amplifier (EA) is proposed that detects the load transient conditions and add extra current to the EA to make it respond vastly to sudden change at the buck output. This idea depends on increasing the EA slew-rate. It is known that the slew-rate of EA can help in minimizing the transient time for buck converter, but this is true if the buck converter output capacitor is large enough to overcome the disturbance happened at the output. If the output capacitor value is already small, the EA slew-rate will not be useful at this moment.

Rather than increasing the EA slew-rate, our novel linear-nonlinear control technique is to saturate the EA output at values near the supply voltage (VDD) or ground voltage (GND) during output undershoot or overshoot respectively. The basic circuit of our idea is shown at Fig. 5-2.

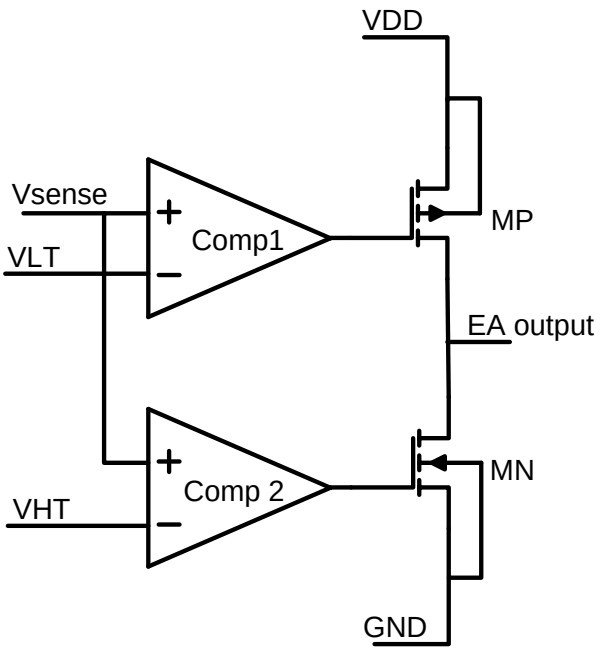


Figure 5-2: The basic circuit of proposed idea.

In the circuit shown in Fig. 5-2, we have two comparators and two transistors. The two transistors have their drains connected together and tied by the EA output. The two comparators are used to detect the buck output's undershoot and overshoot. The detection is reached by comparing *Vsense* node with two threshold levels *VTL* and *VTH* where:

- *Vsense: is a scaled version of the buck output.*
- *VTL: is the low threshold level.*
- *VTH: is the high threshold level.*

During steady-state operation we have two conditions. The first condition is step-up load change (from no-load to full-load) and during this the buck output will undershoot. The second condition is step-down load change (from full-load to no-load) and during this the buck output will overshoot. The operation of the proposed linear-nonlinear technique can be described as follows:

Step-up load change condition:

The buck output undershoots due to the rapid change from no-load to full-load. The *Vsense* is a scaled version from the buck output, so *Vsense* undershoots too. When *Vsense* undershoots it becomes smaller than *VLT* and the corresponding comparator output go low. This will turn on the PMOS transistor *MP*. When *MP* turns on, this pulls the EA output up to values near VDD. Saturating the EA output to high values will force the duty-cycle to be high until the buck output recover to its steady-state value. The recovery of

buck output makes Vsense recover too, and the NCT is turned-off again. This operation is indicated at Fig. 5-3.

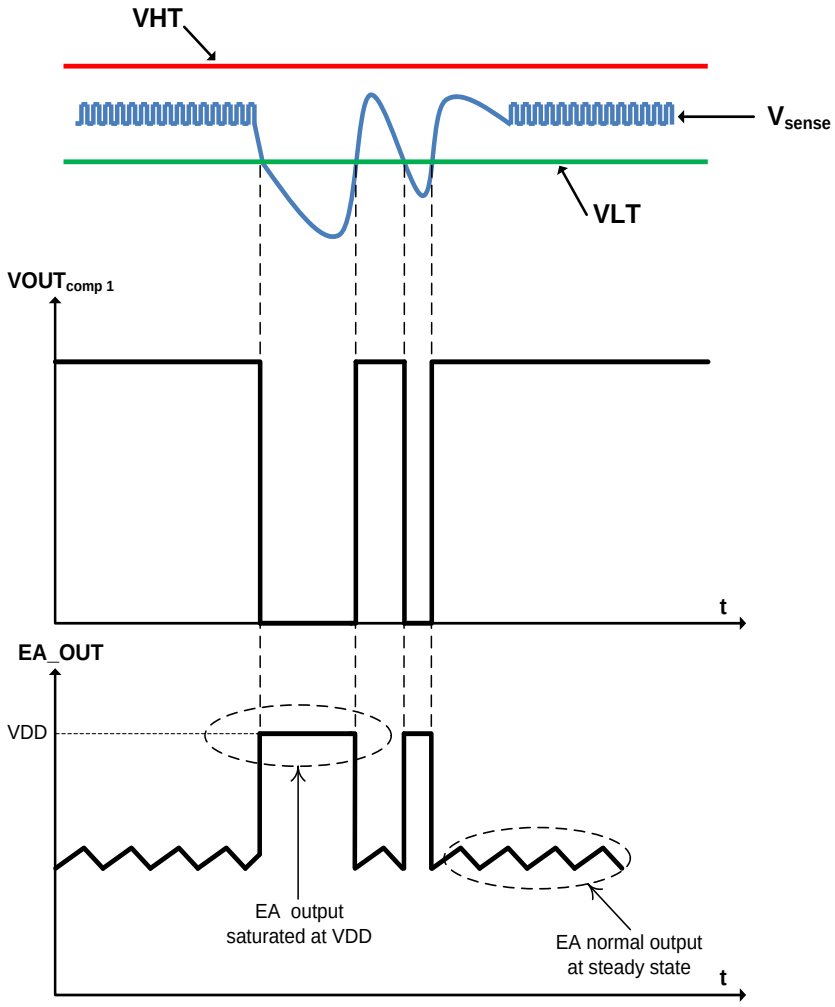


Figure 5-3: Effect of nonlinear technique during buck output's undershoot.

Step-down load change condition:

The buck output overshoots due to the rapid change from full-load to no-load. By the same way, Vsense overshoots too. When Vsense overshoots, it becomes higher than VHT and the corresponding comparator output goes high. This will turn-on the NMOS transistor MN. When MN turns-on, this

pulls the EA output down to values near GND. Saturating the EA output to very low values will force the duty-cycle to be low until the buck output recovers to its steady-state value and the NCT is turned off again. This operation is indicated at Fig. 5-4.

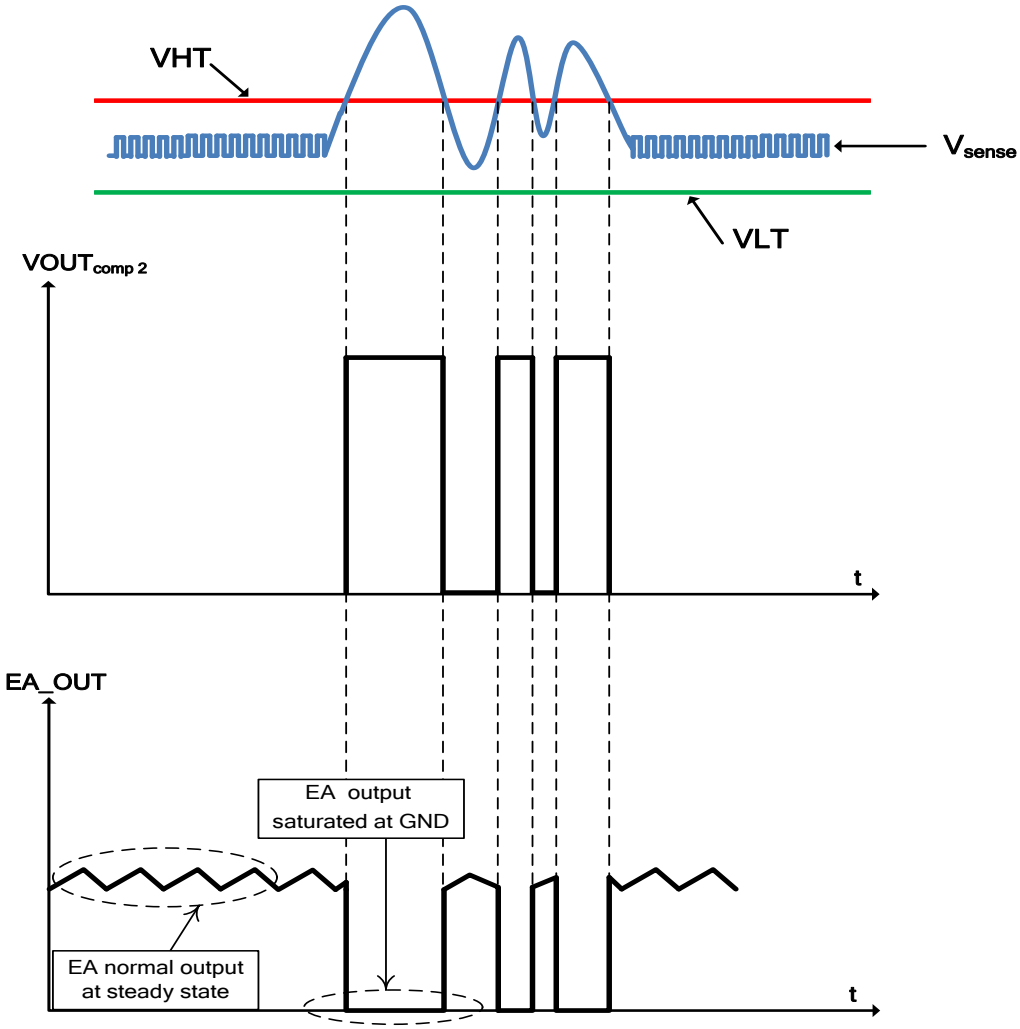


Figure 5-4: Effect of nonlinear technique during buck output's overshoot.

5.3 The Design of Nonlinear Operation Monitoring System

If the nonlinear control technique is left without monitoring, it could continue in operation by fault and make the buck output oscillate which affects the buck stability. The need of a system that monitors the technique and controls its operation is necessary. The proposed nonlinear operation monitoring (NOM) system is used to monitor the nonlinear control technique and disable it, if it continues in operation for a long time. The block diagram of the NOM system is shown in Fig. 5-5. The main core of the NOM system is: one-shot circuit, delay, and OR gate.

The operation of the NOM system can be described for undershoot event; as an example; as the following:

- During steady-state operation of buck converter the *Vsense* voltage is higher than the low threshold voltage *VLT*. The comparator Comp1 output is high, this make the transistor MP turned off.

- When Comp1 detects that there is undershoot at the buck output, its output goes low after it was high. If the nonlinear technique continues in operation, the output of Comp1 will be as shown in Fig. 5-5.

- The Comp1 output is inverted and applied to a one-shot circuit that convert the oscillating signal to one-shot signal. Then the one-shot signal is delayed by a period equal 10 us to give the chance to nonlinear technique to recover without a help. If it doesn't recover, the OR logic

will sum the delayed one-shot signal with the Comp1 output to force it go back to high state.

The same operation is applied for Comp2 during overshoot event. But, the overshoot's NOM circuit uses AND gate instead of OR gate to control the operation of transistor MN.

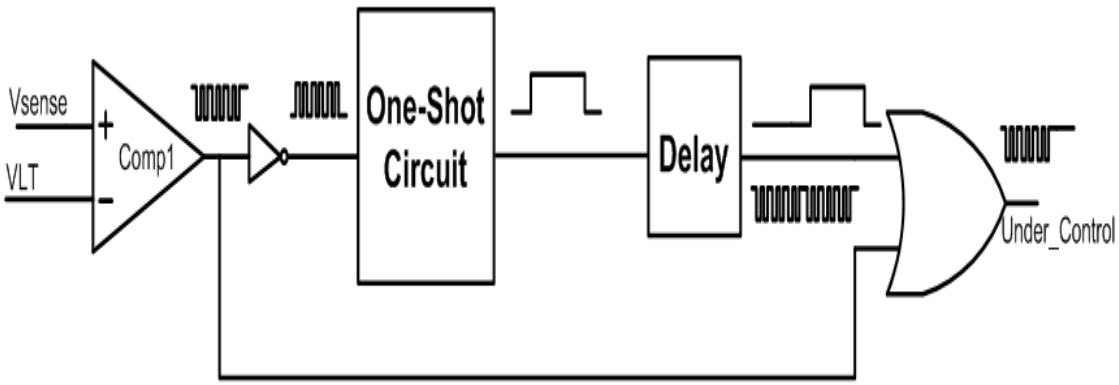


Figure 5-5: The block diagram of nonlinear operation monitoring system (NOM).

5.4 Test and Simulation of The Nonlinear Control Technique

The linear-nonlinear control technique is applied for the designed buck converter that is discussed in details at Chapter 4. For testing the technique, the designed buck converter has been simulated at the following conditions:

- Input voltage = 3 V.
- Output Voltage= 1 V.
- Switching frequency= 2 MHz.
- Output current = 3A.

The buck inductor value is chosen to be 220nH inductor. We choose more than one output capacitor to test our technique. The selected output capacitors data are shown in Table I. The data are taken at the switching frequency 2MHz using ceramic capacitor electrical characteristics from Kyocera [6].

Table 5-1: The output capacitors ESR and ESL values

Capacitor Value	Capacitor ESR	Capacitor ESL
10µF	10 mΩ	0.3 nF
22µF	4 mΩ	0.55 nF
47µF	8 mΩ	0.9 nF
100µF	5 mΩ	0.8 nF

The ESR and Impedance Vs. frequency plot and ESL Vs. frequency plot are shown in Fig. 5-6 and Fig. 5-7, respectively.

The selected output capacitors are small in footprint and have X5R dielectric type. This dielectric type doesn't lose a lot of capacitance with increasing the frequency or changing the biasing conditions. Generally, ceramic capacitors are able to operate over a wide temperature range and have extremely low Equivalent Series Resistance (ESR) and inductance when compared to other technologies such as tantalum or electrolytic components. The lower the ESR and inductance, the more efficient the component will be.

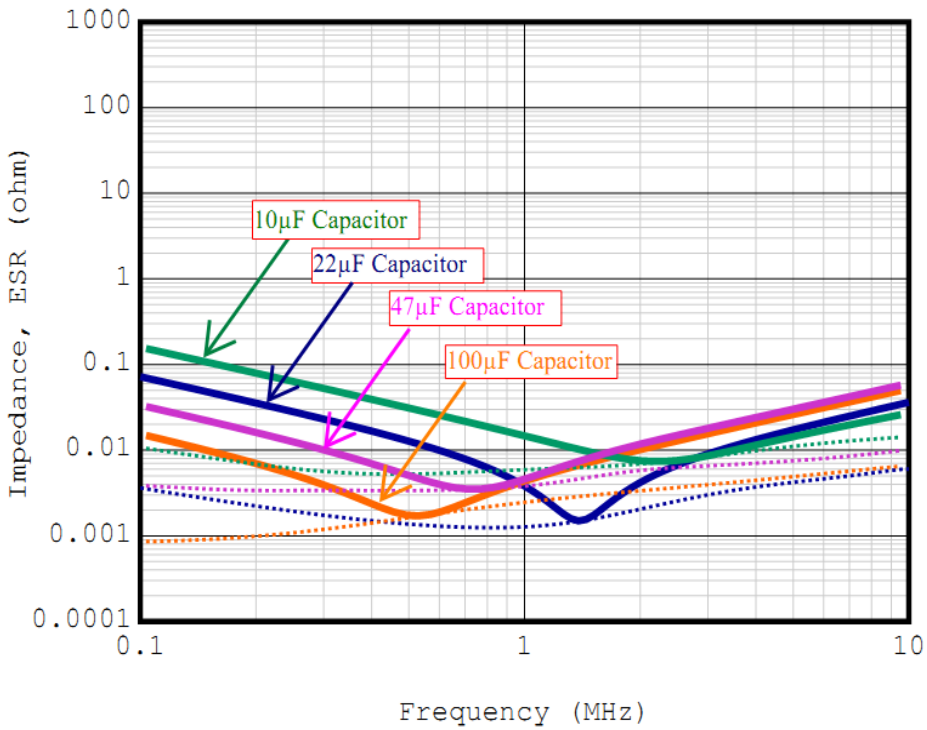


Figure 5-6: Impedance and ESR of ceramic output capacitors [37].

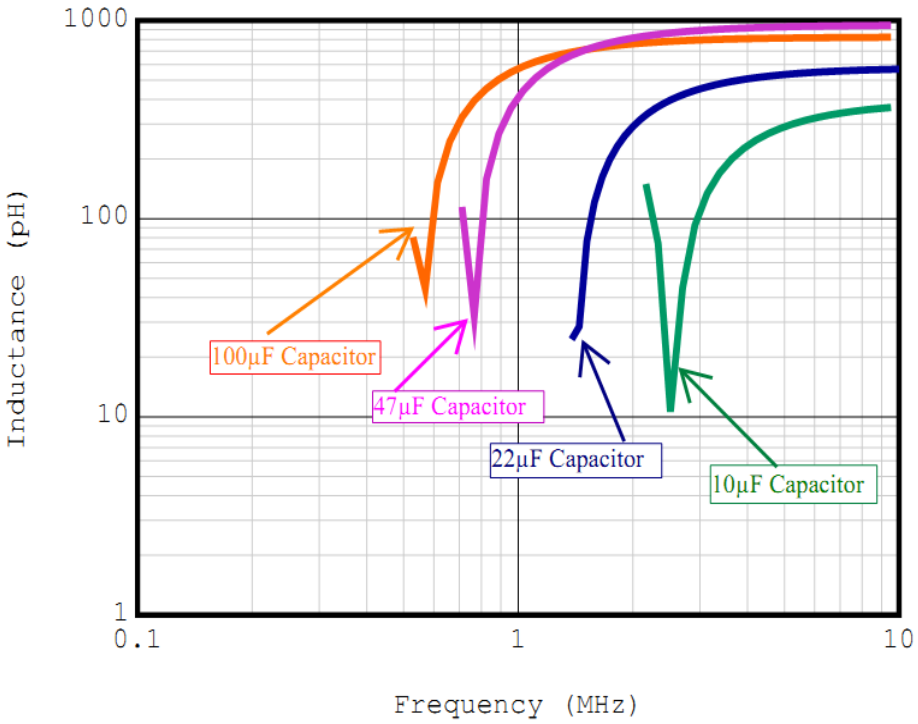


Figure 5-7: ESL of ceramic output capacitors [37].

The proposed technique is applied at the designed buck converter and a load change from 0 A to 3 A has been studied. The slew rate of the output current affects the deviation happen at the output voltage. This mean that if we increased the slew rate very much, a higher output voltage undershoot and overshoot will result. Modern microprocessors are going very fast from sleep mode (very low current loading on buck) to full mode (full load current loading on buck). This mean that the buck output load can be changed from no-load to full-load in very small time measured in nano-second. Our designed technique is test at relatively high output current slewing equal 0.1A/ns. So, our buck converter is loaded by output current that go from 0 A to 3 A in 30 ns which is a very high slew rate compared market examples.

Fig. 5-8 shows the simulation results for the buck output using the proposed technique. The EA output and the output current change are shown at the same figure.

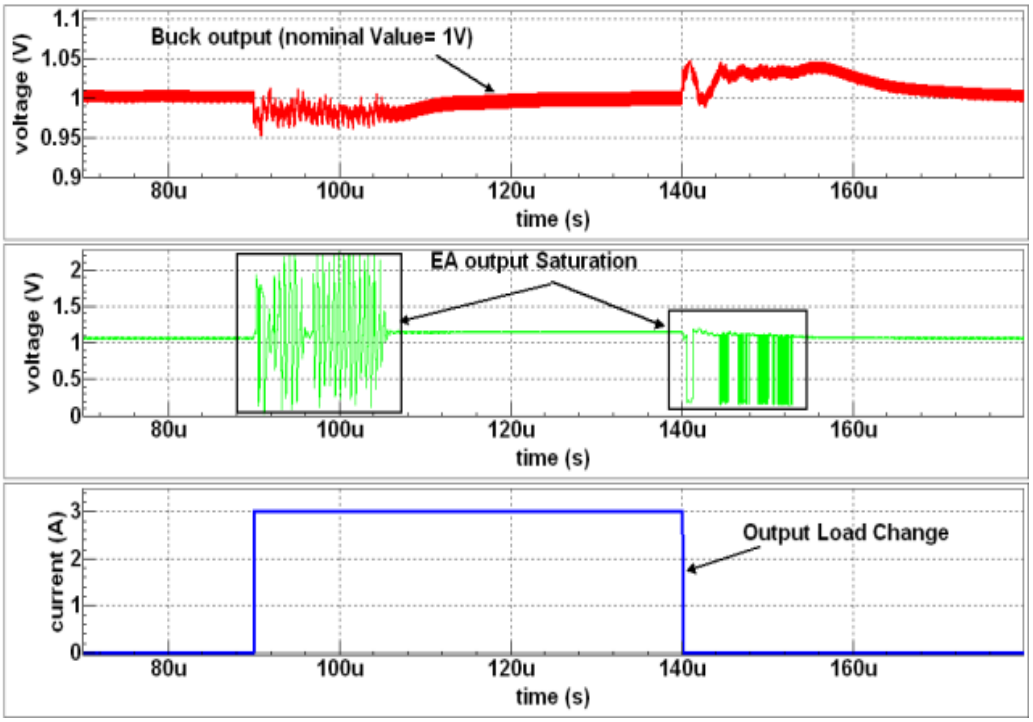


Figure 5-8: Simulation results of buck output, EA output, and output load using the proposed technique.

For comparison and validating the proposed technique, Fig. 5-9 shows the buck output with conventional linear VM control and with the proposed LNL control. It shows the advantage of our proposed control.

The operation of the nonlinear-operation-monitoring (NOM) circuit is tested. It shows a very good result based on our expectation that nonlinear technique continued in operation for long time. This condition is shown in Fig. 5-10.

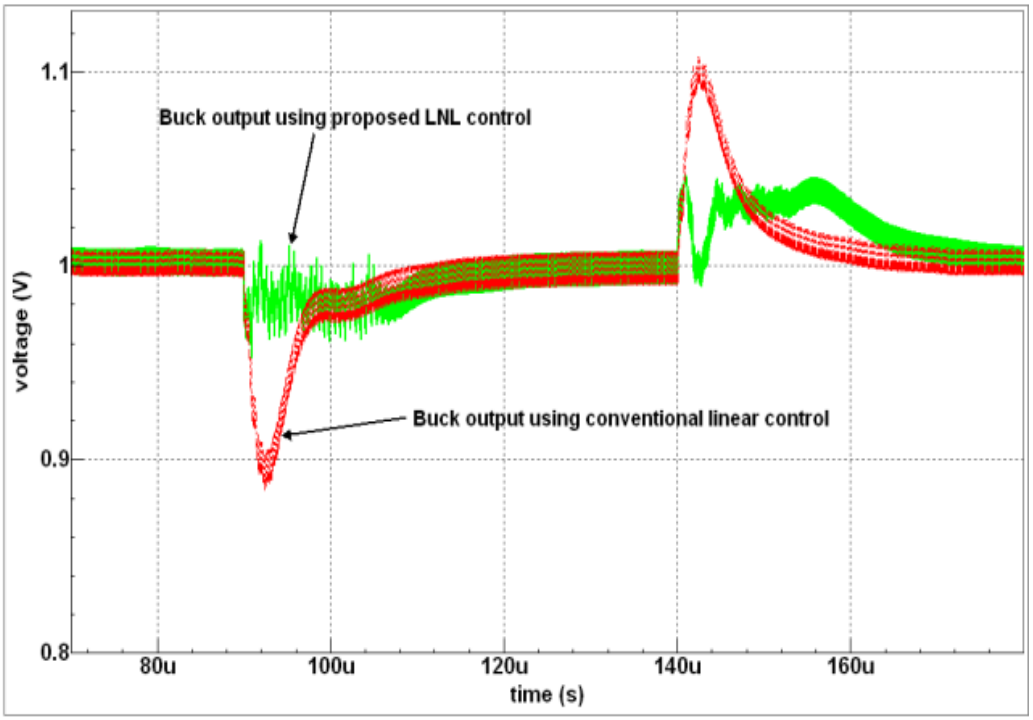


Figure 5-9: Simulation results of buck output with and without the proposed technique.

In Fig. 5-10, the top chart includes the Vsense signal with the window around it. The bottom chart shows *under_control* signal which is the output of the NOM circuit and the gate signal of MP transistor. It is that when the nonlinear technique continued in operation for 15 us, the NOM circuit output goes back to high state to disable the nonlinear operation. After disabling the nonlinear technique, the conventional linear VM control is sufficient to recover the buck output to its steady-state value.

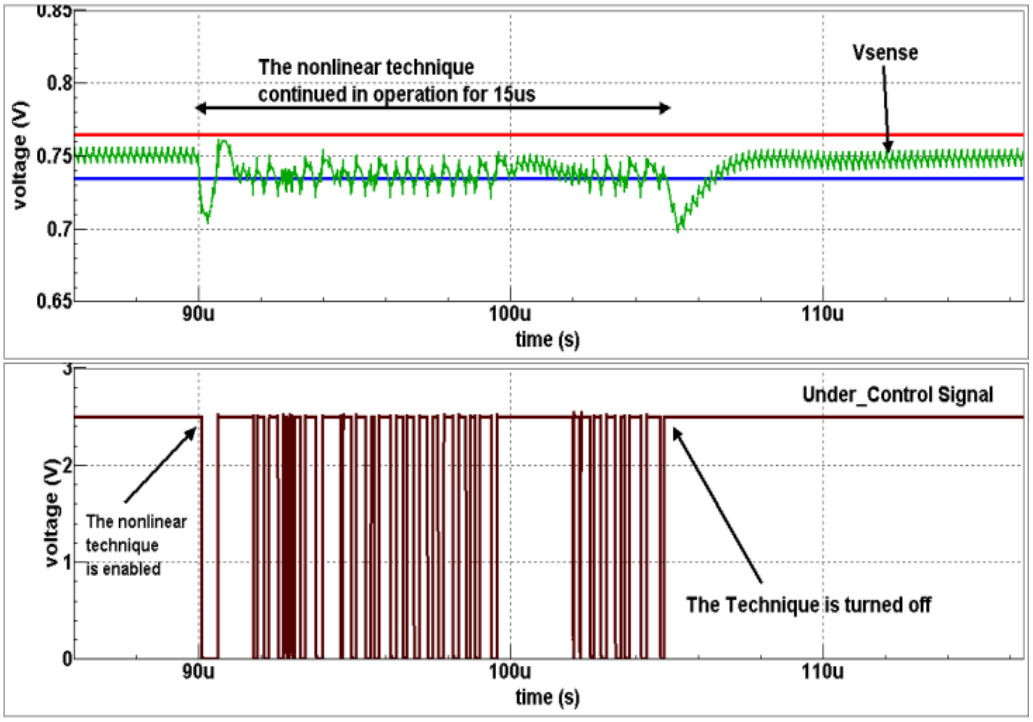


Figure 5-10: Simulation results of NOM circuit.

For showing the advantage of our novel linear-nonlinear technique, a comparison between undershoot and overshoot percentages using the conventional linear control and the proposed LNL technique is presented at Table 5-2.

Table 5-2: Undershoot and overshoot percentages with and without LNL technique

Output Capacitor Value	The Conventional Linear VM	The proposed LNL technique
47 µF (ESL=1.5 n, ESR=2 m) +10 u (ESL=0.9 n, ESR=1.5 m)	Undershoot =10.6%	Undershoot =3.9%
	Overshoot =10.1%	Overshoot = 4%
2X 12 µF (ESL=0.7 n, ESR=2 m)	Undershoot =11.6%	Undershoot = 4.5%
	Overshoot = 11.1%	Overshoot = 5.2%
12 µF (ESL=0.7 n, ESR=2 m)	Undershoot = 12.2%	Undershoot =6.9%
	Overshoot =12%	Overshoot = 4.8%

It is clear from Table 5-2 that the proposed technique reduces undershoot and overshoot percentage by at least 4%. This makes our proposed technique useful for the applications that are sensitive for output voltage large deviation.

It is possible to get the same undershoot and overshoot percentage using the conventional linear VM control but using smaller output capacitor. According to the results shown in Table 5-1, we can replace the combination of 47 µF and 7 µF with a one 12 µF output capacitor. Undershoot and overshoot percentage is still smaller than the first case that of the conventional linear VM control.

The proposed technique is totally off during normal operation of buck converter and is enabled only during load transient and output disturbances. So, it has no effect on the buck efficiency. The power consumption of the LNL technique circuits is very small compared to the output power.

Fig. 5-11 shows the load transient response with the same output capacitor using the linear-nonlinear control that has been proposed. The results show that there is a minimum 5% reduction in undershoot and overshoot percentages.

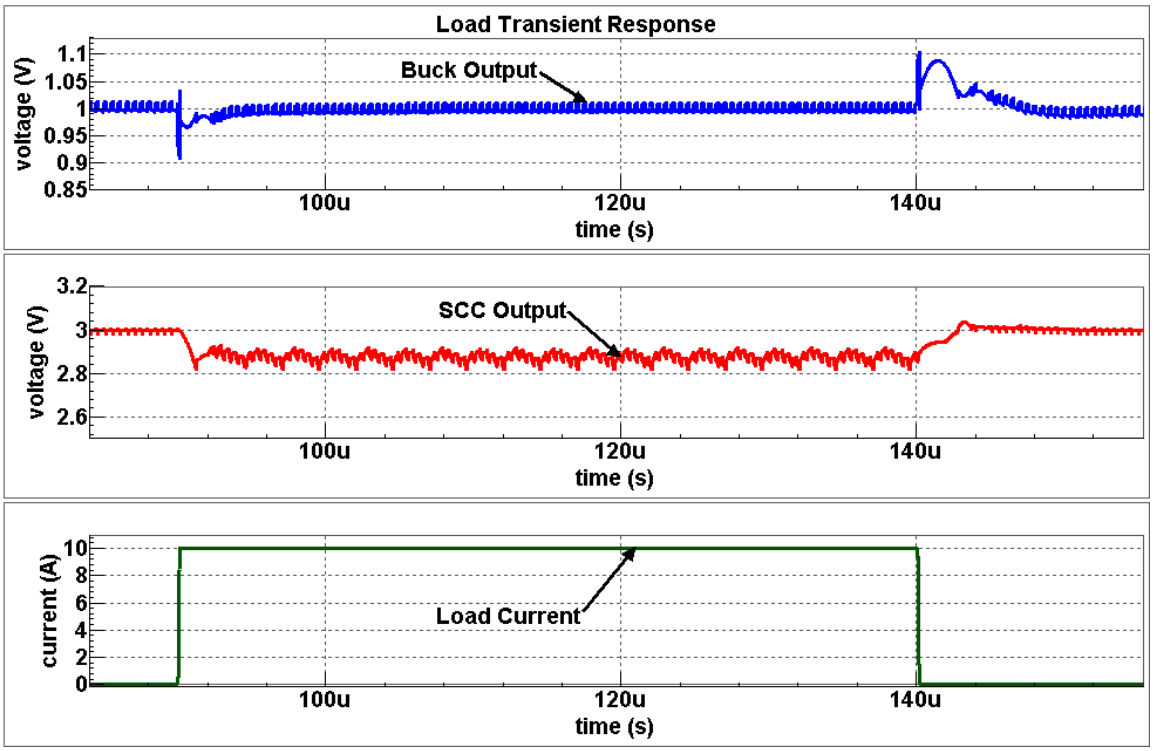


Figure 5-11: Load transient response of the two-stage system with nonlinear control.

5.5 Conclusion

In this chapter, the design of nonlinear control technique for buck converter has been proposed. This technique can be used side-by-side with the conventional linear control. This technique is used mainly to improve the transient response of buck converter during load transient. It is proven by results that the proposed technique can reduce undershoot and overshoot percentages by a minimum value of 4%.

The SCC that is previously designed in chapter three is integrated with the buck converter designed in chapter four to simulate the two-stage system. The simulation result of the integrated two-stage system show that high efficiency can be obtained at high output current. Then, the efficiency of two-stage approach is compared to the one-stage buck converter and the simulation result showed that the two-stage system is better than the buck converter by at least 7%.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

There is a rapid evolution in portable devices market and wide variety of consumer electronics is developed each year. These consumer electronics are going faster and smaller to satisfy the user needs. In order for these devices to perform faster in addition to being smaller, the semiconductor chips are scaled down to cover the size requirements in the market. In addition, the number of transistors per chip is increasing rapidly as Moore's law predicted. The enormous number of transistors per chip requires more power and for this reason the semiconductor chips available nowadays consume more power.

Voltage regulator that supplies the semiconductor chips should be able to satisfy the high power requirements for such chips. The issue is not in supplying such chips with the required power, the most important issue is the efficiency of conversion. These regulators should be efficient to extend the battery life. In addition to being efficient, these regulators should be small in size to save the PCB area and to be embedded at light portable devices. Minimum number of external components should be used to reduce the cost of the solution.

This thesis introduced new power architecture for low-power processor applications. The two-stage architecture can replace the conventional one-stage approach for processor's power supply.

The thesis began with a study for the power supply topologies available in the market and investigation for the advantages and disadvantages of each topology has been illustrated. The available power architectures for low-power processors are investigated and the new power architecture has been

discussed. The topology of each stage in the new two-stage power supply has been selected.

The topology used in each stage has been explained in details. The operation theory of switched-capacitor converter has been explained and followed by the design of power-stage of the converter. For proper operation, the design of sub-blocks of the converter has been shown and the simulation results of the switched-capacitor converter have been illustrated.

The operation theory of buck converter has been explained and the use of this converter as a second-stage for our power supply has been discussed. The PWM controller of buck converter has been employed and the design of the controller sub-blocks has been discussed in details. Simulation result for the integration of the buck converter and its controller has been illustrated. The results prove that lower input voltage increases the efficiency of buck converter.

The switched-capacitor converter has been integrated with the buck converter to compose the two-stage power supply. The total system has been simulated and the efficiency of the system has been illustrated, In comparison with the one-stage approach, the two-stage power supply shows that higher efficiency by at least 7% can been obtained using the new architecture.

To satisfy the high slew-rate requirements of current processors, a new nonlinear technique has been proposed. This new technique can be integrated with the conventional linear control technique to operate only during the output transient. The simulation results show that undershoot and overshoot can be effectively reduced using this new technique.

6.2 Future Work

During the work in this thesis, there are many research work can be studied in future work. Some of these points are as follow.

1- *Different techniques used to decrease the losses of buck converter at light loads.*

It is known from previous efforts and analyses that the POL buck converter suffers a lot at light loads due to the increase in switching loss which becomes significant. One possible solution is to operate the buck converter in PFM mode at light loads. The problem in PFM operation is the output ripples which become unpredictable. Future work can involve the proposing of a new technique or a hybrid technique to reduce the switching loss of buck converter at light loads.

2- *Design of low cost, efficient, and small size power supply for PA used in modern smart phones.*

Designing a power supply for PAs is totally different than that of microprocessors. The first one is noise sensitive which make the buck converter a bad choice for such applications. One brilliant choice is to use linear regulators to power the blocks of PA. In smart phones, the Lithium-ion batteries are the source of energy. The battery voltage changes between 4.2 V to 3.7 V depending on the charge state of the battery. Cascading a step-up/step-down switched capacitor converter followed by a linear regulator would be more advantageous from the efficiency and cost point of view.

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تم تصنيع المرحلة الاولي من مصدر القدرة باستخدام تكنولوجيا شبه موصل أكسيد الفلز وتم اخذ نتائج معملية. النتائج المعملية أظهرت ان الكفاءة التي يمكن الحصول عليها من المرحلة الاولي اعلي من 90%.

وأخيرا, تم تجميع مرحلتي محول الجهد ومحاكاتها وحساب كفاءة المحول الجديد ذو المرحلتين. وبمقارنة كفاءة المحول ذو المرحلتين مع كفاءة المحول ذو المرحلة الواحدة , أوضحت النتائج أن المحول ذو المرحلتين أعلي كفاءة وأقل سعرا.

الملخص العربي

تصميم الدوائر المتكاملة لمحولات الجهد المستمر عالية الأداء لتطبيقات معالج منخفض القدرة

خلال ساعات يومنا هناك عدد كبير من الأجهزة الإلكترونية التي نستخدمها. معظم هذه الأجهزة محمولة وتعمل بواسطة بطاريات ليثيوم-أيون. ويمكن في هذه الأيام يمكن العثور على كل هذه الأجهزة مدمجة في جهاز واحد الذي يمكن اعتباره جهاز متعدد الوظائف. العديد من هذه الأجهزة تشتمل علي رقائق مصنعة بتكنولوجيا أشباه-الموصلات الأكثر تطورا. مثال لهذه الرقائق هي المعالجات الدقيقة. المعالجات الدقيقة تكون محملة بكثير من المهام والوظائف أكثر من أي شريحة أخرى في الأجهزة المحمولة. الاتجاه الحالي في السوق هو خفض جهد المصدر لهذه المعالجات لإدارة طاقتها بفاعلية. إضافة إلى ذلك، فإن زيادة وظائف هذه المعالجات يجعلها في حاجة لتياركهربي أعلي. كل هذا يضع مزيد من التحديات أمام تصميم مصادر القدرة لهذه المعالجات.

إنه من الضروري لمصمم مصادر القدرة لهذه المعالجات أن يحسن من كفاءة مصدر القدرة للحفاظ علي الطاقة وإطالة عمر البطارية. ورغم أن كفاءة مصدر القدرة يعتبر مطلب حيوي , إلا ان حجم وتكلفة مصدر القدرة من الامور المهمة التي يجب أن تؤخذ في الحسبان.

هذه الدراسة تعطي لمحة عن أهمية مصادر القدرة للمعالجات الحديثة وأنواع منظمات الجهد المتاحة في السوق. تم تقديم دراسة عن أبنية إدارة الطاقة للمعالجات ثم إقتراح تصميم محول جهد ذو مرحلتين لاستخدامه بدلا من محول الجهد ذو المرحلة الواحدة.

تم مناقشة تصميم كل مرحلة لمحول الجهد المقترح بالإضافة الي الي تقديم كيفية تصميم دوائر التحكم الخاصة بهذه المراحل. بعد ذلك تم محاكاة كل مرحلة علي إنفراد وعرضت النتائج.

من أجل إستجابة وقتية أسرع , تم إقتراح تقنية تحكم خطية-غير خطية جديدة لتحسين إستجابة الخرج الوقتية في حالة التغير الوقتي المفاجئ للحمل.

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تصميم الدوائر المتكاملة لمحولات الجهد المستمر عالية الأداء لتطبيقات معالج منخفض القدرة

رسالة من إحدى متطلبات الحصول على درجة الماجستير فى الهندسة الكهربية

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